FIG. 1

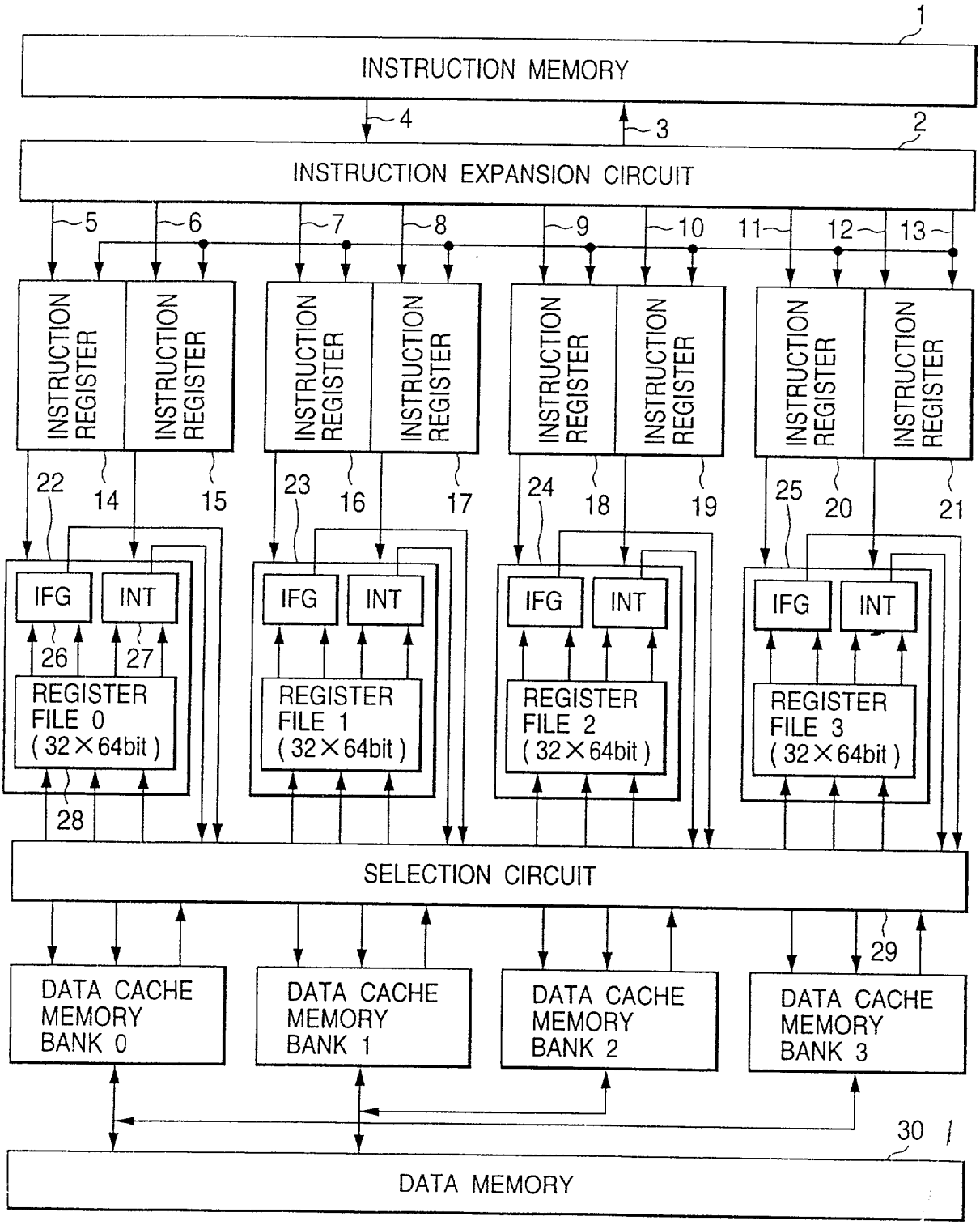
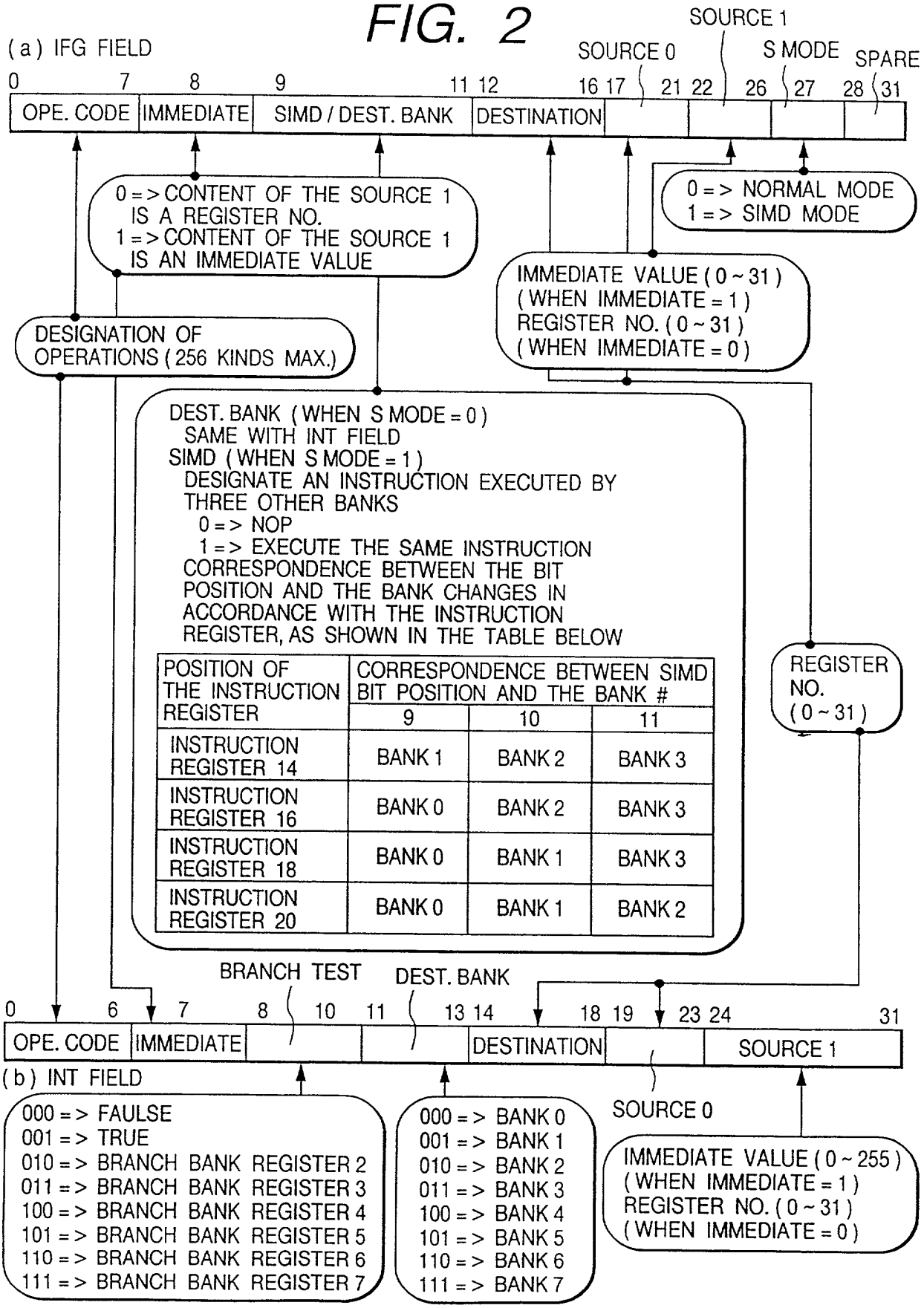

1
INSTRUCTION MEMORY
4
3
2
INSTRUCTION EXPANSION CIRCUIT
5
6
7
8
9
10
11
12
13
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
22
14
15
23
16
17
24
18
19
25
20
21
IFG
INT
IFG
INT
IFG
INT
IFG
INT
26
27
REGISTER FILE 0 (32×64bit)
REGISTER FILE 1 (32×64bit)
REGISTER FILE 2 (32×64bit)
REGISTER FILE 3 (32×64bit)
28
SELECTION CIRCUIT
29
DATA CACHE MEMORY BANK 0
DATA CACHE MEMORY BANK 1
DATA CACHE MEMORY BANK 2
DATA CACHE MEMORY BANK 3
30
DATA MEMORY

FIG. 2



POSITION OF THE INSTRUCTION REGISTER	CORRESPONDENCE BETWEEN SIMD BIT POSITION AND THE BANK #		
	9	10	11
INSTRUCTION REGISTER 14	BANK 1	BANK 2	BANK 3
INSTRUCTION REGISTER 16	BANK 0	BANK 2	BANK 3
INSTRUCTION REGISTER 18	BANK 0	BANK 1	BANK 3
INSTRUCTION REGISTER 20	BANK 0	BANK 1	BANK 2

FIG. 3

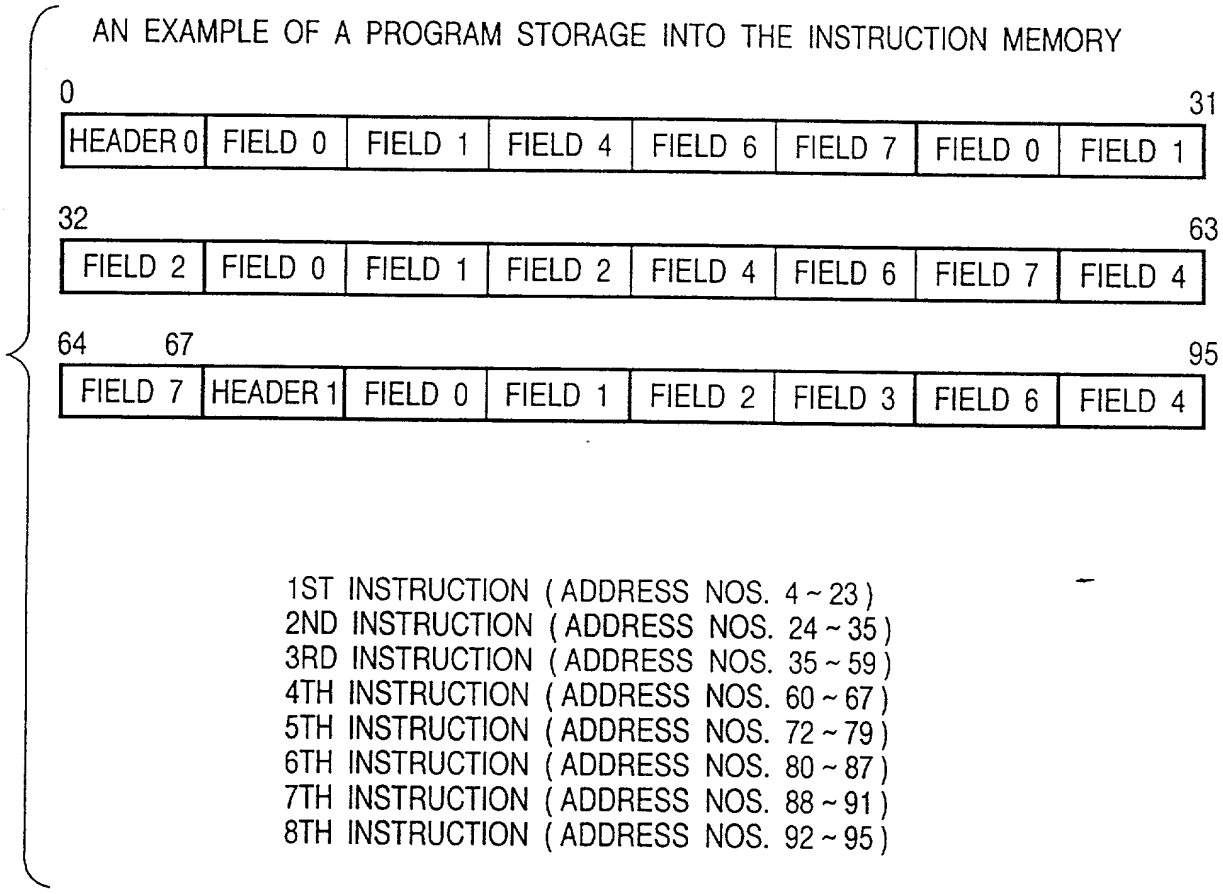

AN EXAMPLE OF A PROGRAM STORAGE INTO THE INSTRUCTION MEMORY
0
31
HEADER 0
FIELD 0
FIELD 1
FIELD 4
FIELD 6
FIELD 7
FIELD 0
FIELD 1
32
63
FIELD 2
FIELD 0
FIELD 1
FIELD 2
FIELD 4
FIELD 6
FIELD 7
FIELD 4
64
67
95
FIELD 7
HEADER 1
FIELD 0
FIELD 1
FIELD 2
FIELD 3
FIELD 6
FIELD 4
1ST INSTRUCTION (ADDRESS NOS. 4 ~ 23)
2ND INSTRUCTION (ADDRESS NOS. 24 ~ 35)
3RD INSTRUCTION (ADDRESS NOS. 35 ~ 59)
4TH INSTRUCTION (ADDRESS NOS. 60 ~ 67)
5TH INSTRUCTION (ADDRESS NOS. 72 ~ 79)
6TH INSTRUCTION (ADDRESS NOS. 80 ~ 87)
7TH INSTRUCTION (ADDRESS NOS. 88 ~ 91)
8TH INSTRUCTION (ADDRESS NOS. 92 ~ 95)

FIG. 4

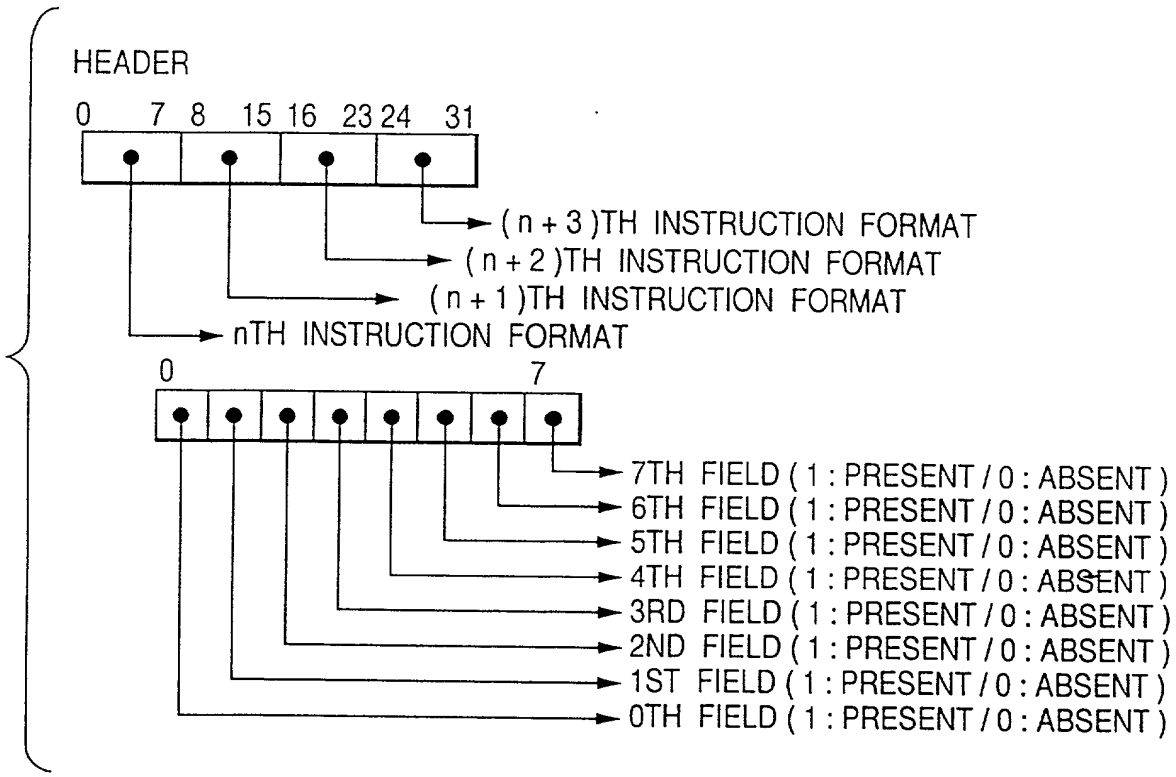

HEADER
0 7 8 15 16 23 24 31
(n+3)TH INSTRUCTION FORMAT
(n+2)TH INSTRUCTION FORMAT
(n+1)TH INSTRUCTION FORMAT
nTH INSTRUCTION FORMAT
0 7
7TH FIELD (1 : PRESENT / 0 : ABSENT)
6TH FIELD (1 : PRESENT / 0 : ABSENT)
5TH FIELD (1 : PRESENT / 0 : ABSENT)
4TH FIELD (1 : PRESENT / 0 : ABSENT)
3RD FIELD (1 : PRESENT / 0 : ABSENT)
2ND FIELD (1 : PRESENT / 0 : ABSENT)
1ST FIELD (1 : PRESENT / 0 : ABSENT)
0TH FIELD (1 : PRESENT / 0 : ABSENT)

FIG. 5

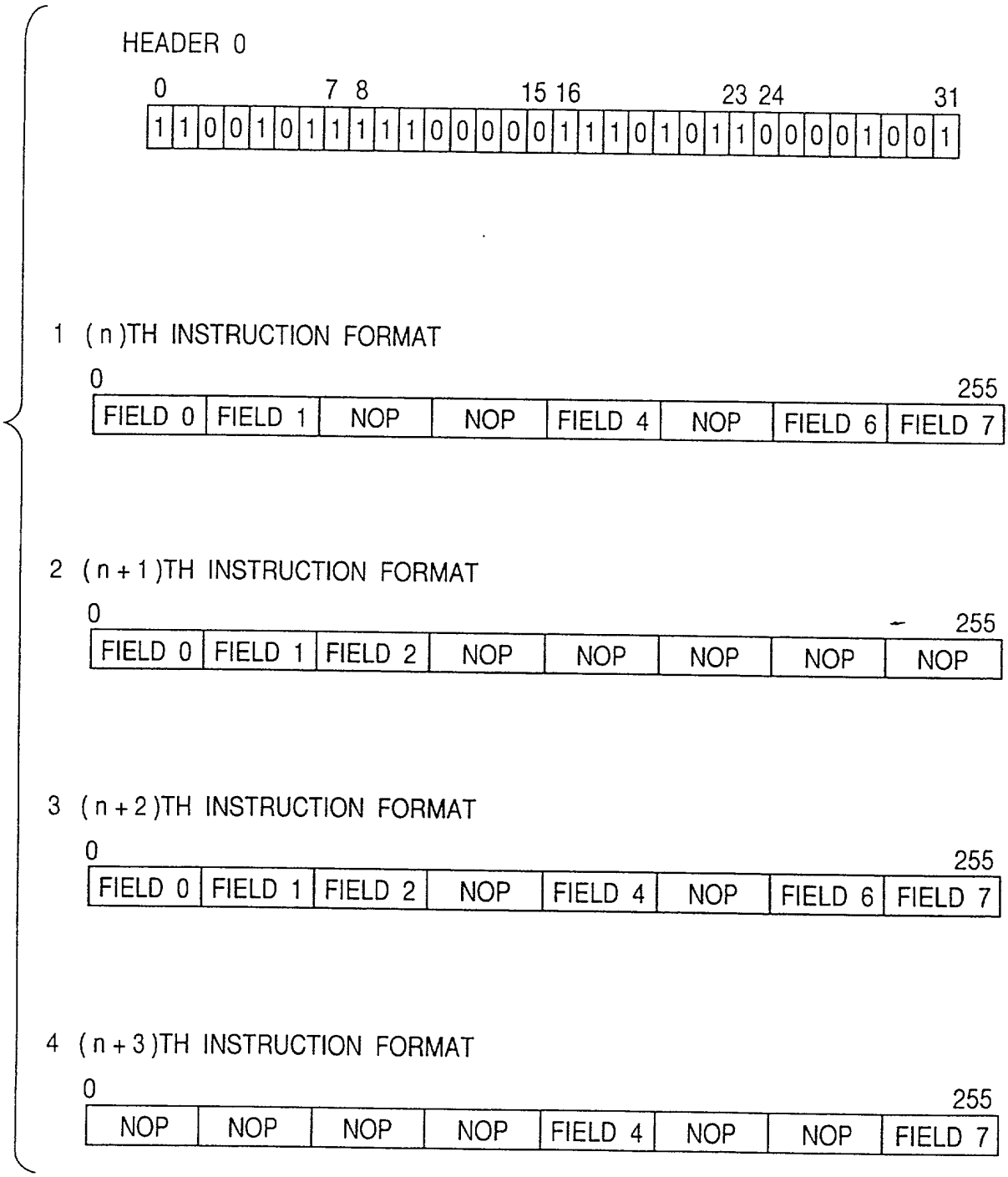

HEADER 0
0
7 8
15 16
23 24
31
1 1 0 0 1 0 1 1 1 1 1 0 0 0 0 0 1 1 1 0 1 0 1 1 0 0 0 0 1 0 0 1
1 (n)TH INSTRUCTION FORMAT
0
255
FIELD 0
FIELD 1
NOP
NOP
FIELD 4
NOP
FIELD 6
FIELD 7
2 (n+1)TH INSTRUCTION FORMAT
0
255
FIELD 0
FIELD 1
FIELD 2
NOP
NOP
NOP
NOP
NOP
3 (n+2)TH INSTRUCTION FORMAT
0
255
FIELD 0
FIELD 1
FIELD 2
NOP
FIELD 4
NOP
FIELD 6
FIELD 7
4 (n+3)TH INSTRUCTION FORMAT
0
255
NOP
NOP
NOP
NOP
FIELD 4
NOP
NOP
FIELD 7

FIG. 6

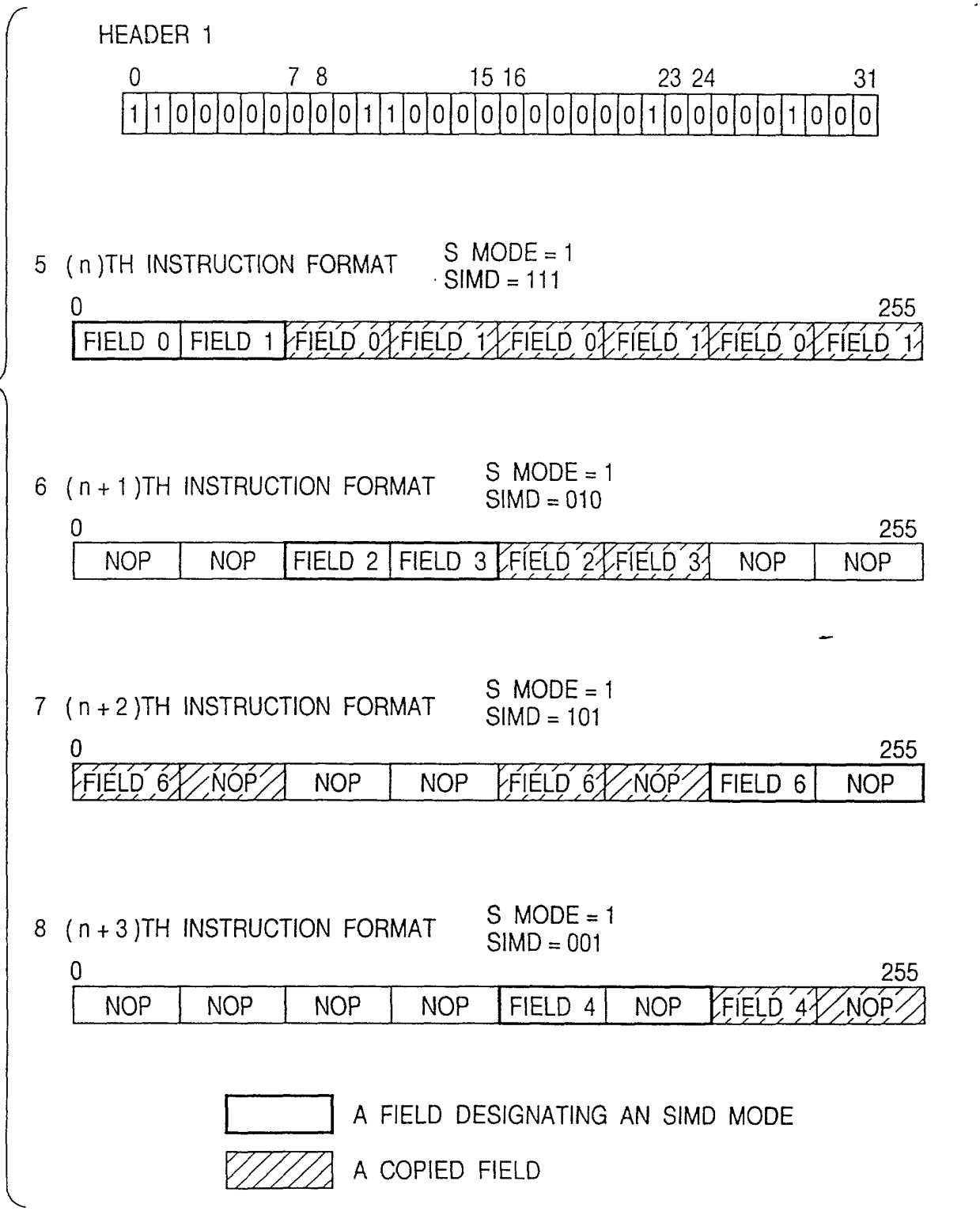

HEADER 1
0 7 8 15 16 23 24 31
1 1 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0
5 (n)TH INSTRUCTION FORMAT
S MODE = 1
SIMD = 111
0 255
FIELD 0 FIELD 1 FIELD 0 FIELD 1 FIELD 0 FIELD 1 FIELD 0 FIELD 1
6 (n+1)TH INSTRUCTION FORMAT
S MODE = 1
SIMD = 010
0 255
NOP NOP FIELD 2 FIELD 3 FIELD 2 FIELD 3 NOP NOP
7 (n+2)TH INSTRUCTION FORMAT
S MODE = 1
SIMD = 101
0 255
FIELD 6 NOP NOP NOP FIELD 6 NOP FIELD 6 NOP
8 (n+3)TH INSTRUCTION FORMAT
S MODE = 1
SIMD = 001
0 255
NOP NOP NOP NOP FIELD 4 NOP FIELD 4 NOP
A FIELD DESIGNATING AN SIMD MODE
A COPIED FIELD

FIG. 7

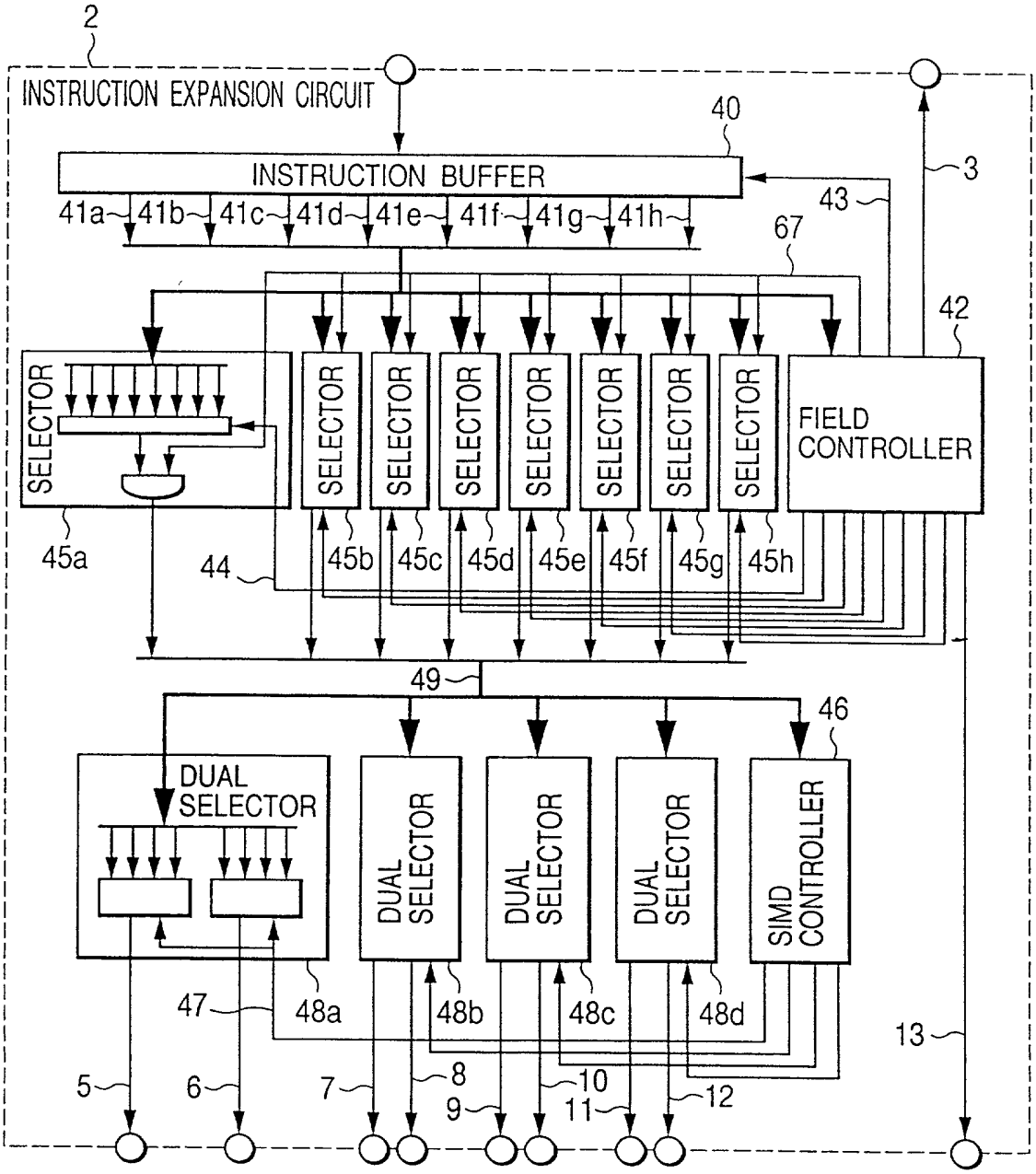

2
INSTRUCTION EXPANSION CIRCUIT
40
INSTRUCTION BUFFER
41a
41b
41c
41d
41e
41f
41g
41h
43
3
67
42
SELECTOR
SELECTOR
SELECTOR
SELECTOR
SELECTOR
SELECTOR
SELECTOR
SELECTOR
FIELD CONTROLLER
45a
44
45b
45c
45d
45e
45f
45g
45h
49
46
DUAL SELECTOR
DUAL SELECTOR
DUAL SELECTOR
DUAL SELECTOR
SIMD CONTROLLER
47
48a
48b
48c
48d
13
5
6
7
8
9
10
11
12

FIG. 8

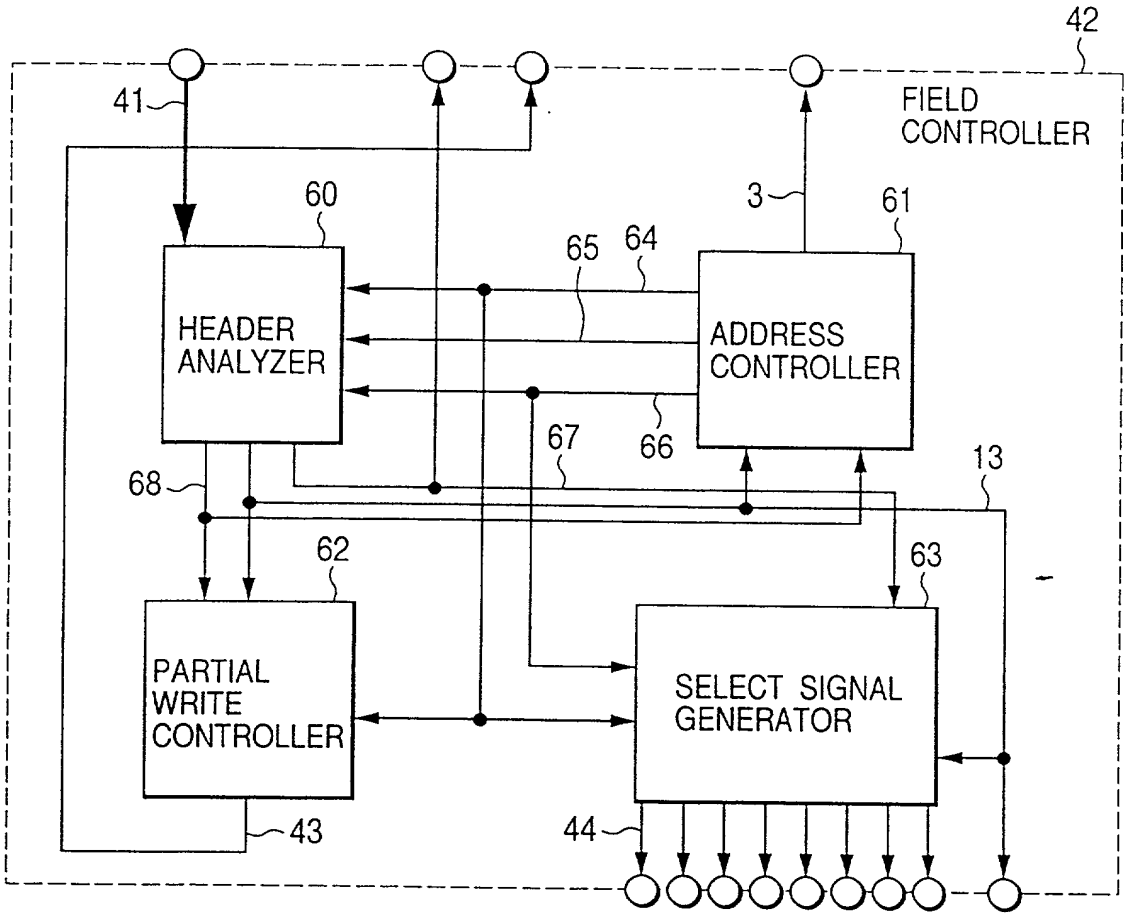

42
41
FIELD CONTROLLER
60
3
61
65
64
HEADER ANALYZER
ADDRESS CONTROLLER
67
66
13
68
62
63
PARTIAL WRITE CONTROLLER
SELECT SIGNAL GENERATOR
43
44

FIG. 9

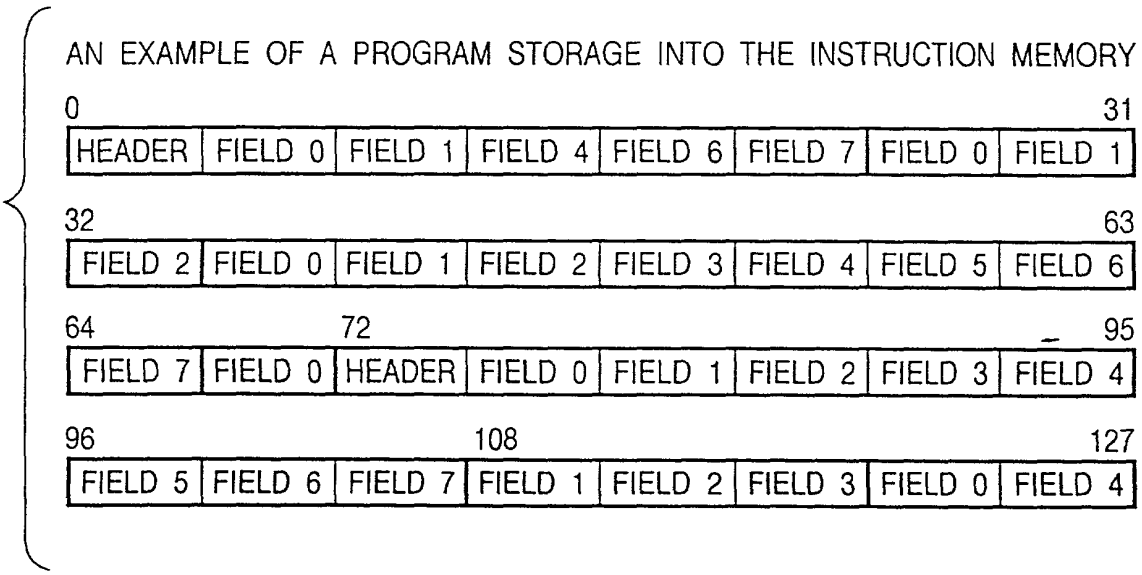

AN EXAMPLE OF A PROGRAM STORAGE INTO THE INSTRUCTION MEMORY
0
31
HEADER
FIELD 0
FIELD 1
FIELD 4
FIELD 6
FIELD 7
FIELD 0
FIELD 1
32
63
FIELD 2
FIELD 0
FIELD 1
FIELD 2
FIELD 3
FIELD 4
FIELD 5
FIELD 6
64
72
95
FIELD 7
FIELD 0
HEADER
FIELD 0
FIELD 1
FIELD 2
FIELD 3
FIELD 4
96
108
127
FIELD 5
FIELD 6
FIELD 7
FIELD 1
FIELD 2
FIELD 3
FIELD 0
FIELD 4

FIG. 10

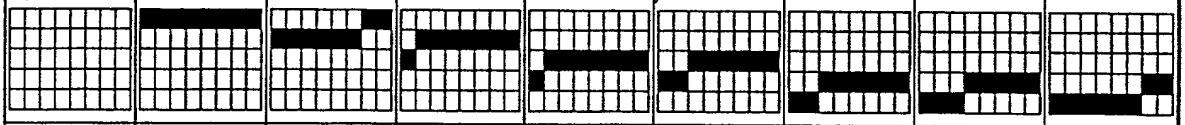
T0	T1	T2	T3	T4	T5	T6	T7	T8
IF	EXP	EXE	WB	INSTRUCTION 1				
	IF	EXP	EXE	WB	INSTRUCTION 2			
	INSTRUCTION 3	IF	EXP	EXE	WB			
		INSTRUCTION 4	IF	EXP	EXE	WB		
			INSTRUCTION 5	IF	EXP	EXP2	EXE	WB
				INSTRUCTION 6		IF	EXP	EXE
REFETCH SIGNAL LINE 13								
0	0	0	0	0	0	1	0	0
INSTRUCTION LENGTH SIGNAL LINE 68								
0	24	12	32	4	36	0	12	8
INSTRUCTION ADDRESS BUS 64								
0	0	24	36	68	72	108	108	120
ADDRESS BUS 3								
0	32	56	68	100	104	136	140	152
WRITE ENABLE BUS 43								
11111111	11111100	10000011	11111111	01000000	11111111	00100000	00011100	00000011
DATA LATCHED IN THE INSTRUCTION BUFFER40 (INDICATED IN CORRESPONDENCE WITH FIG.9)								
								
HEADER ADDRESS BUS 65								
0	0	1	2	3	0	1	1	2
FIELD 0 (SELECT SIGNAL 44)								
0	1	6	1	1	3	-	-	6
FIELD 1	2	7	2	-	4	-	3	-
FIELD 2	-	0	3	-	5	-	4	-
FIELD 3	-	-	4	-	6	-	5	-
FIELD 4	3	-	5	-	7	-	-	7
FIELD 5	-	-	6	-	0	-	-	-
FIELD 6	4	-	7	-	1	-	-	-
FIELD 7	5	-	0	-	-	2	-	-

FIG. 11

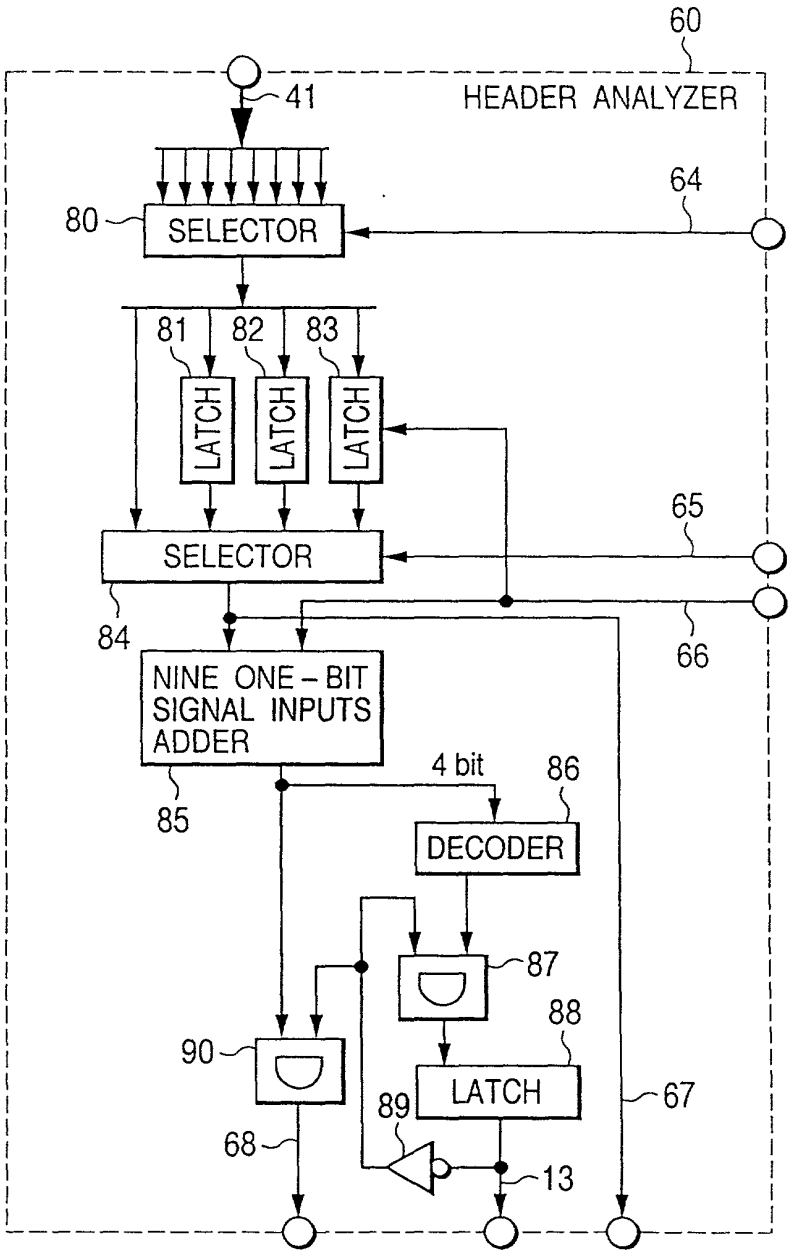
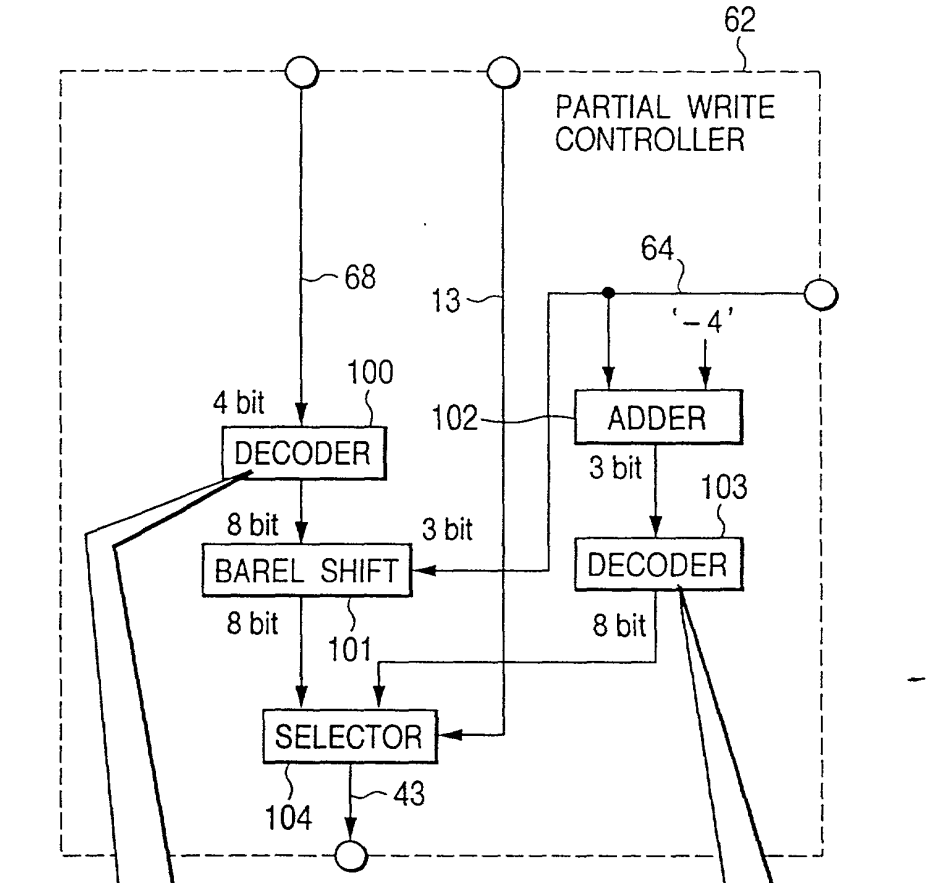

60
HEADER ANALYZER
41
64
80
SELECTOR
81
82
83
LATCH
LATCH
LATCH
65
SELECTOR
84
66
NINE ONE-BIT SIGNAL INPUTS ADDER
85
4 bit
86
DECODER
87
88
90
LATCH
89
67
68
13

FIG. 12



INSTRUCTION LENGTH BUS 68	OUTPUT OF DECODER 100
0001	1000 0000
0010	1100 0000
0011	1110 0000
0100	1111 0000
0101	1111 1000
0110	1111 1100
0111	1111 1110
1000	1111 1111

OUTPUT OF ADDER 102	OUTPUT OF DECODER 103
000	1000 0000
001	1100 0000
010	1110 0000
011	1111 0000
100	1111 1000
101	1111 1100
110	1111 1110
111	1111 1111

FIG. 13

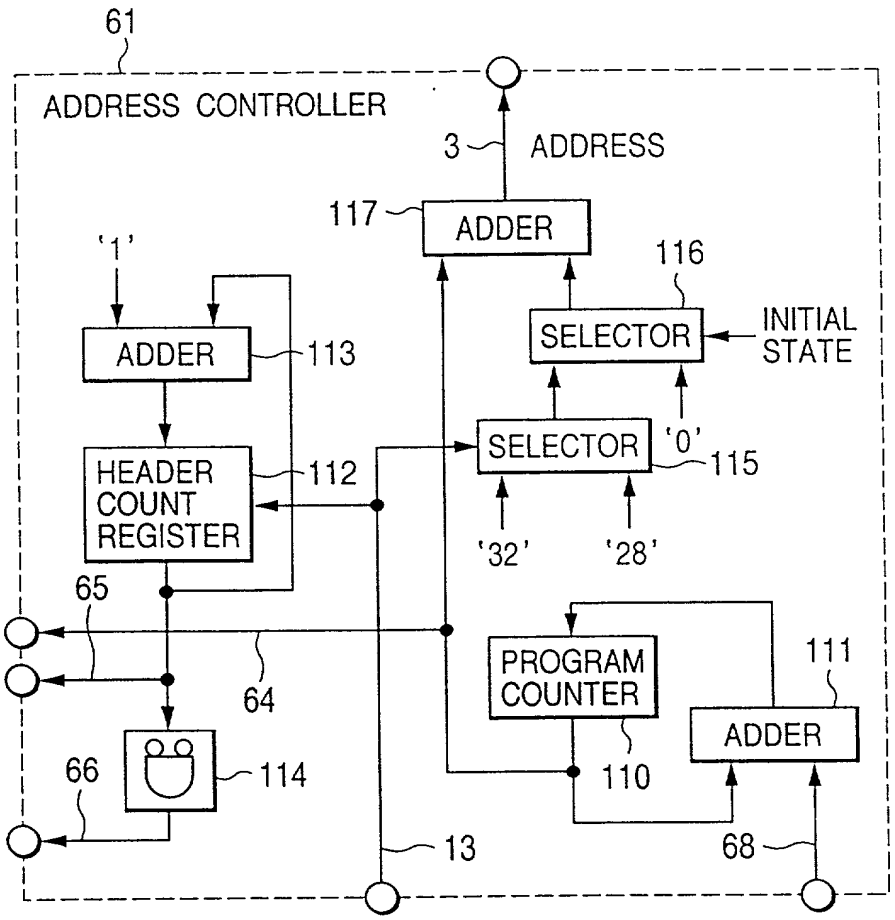

61
ADDRESS CONTROLLER
3
ADDRESS
117
ADDER
'1'
116
SELECTOR
INITIAL STATE
ADDER
113
SELECTOR
'0'
115
HEADER COUNT REGISTER
112
'32'
'28'
65
PROGRAM COUNTER
111
64
ADDER
66
114
110
13
68

FIG. 14

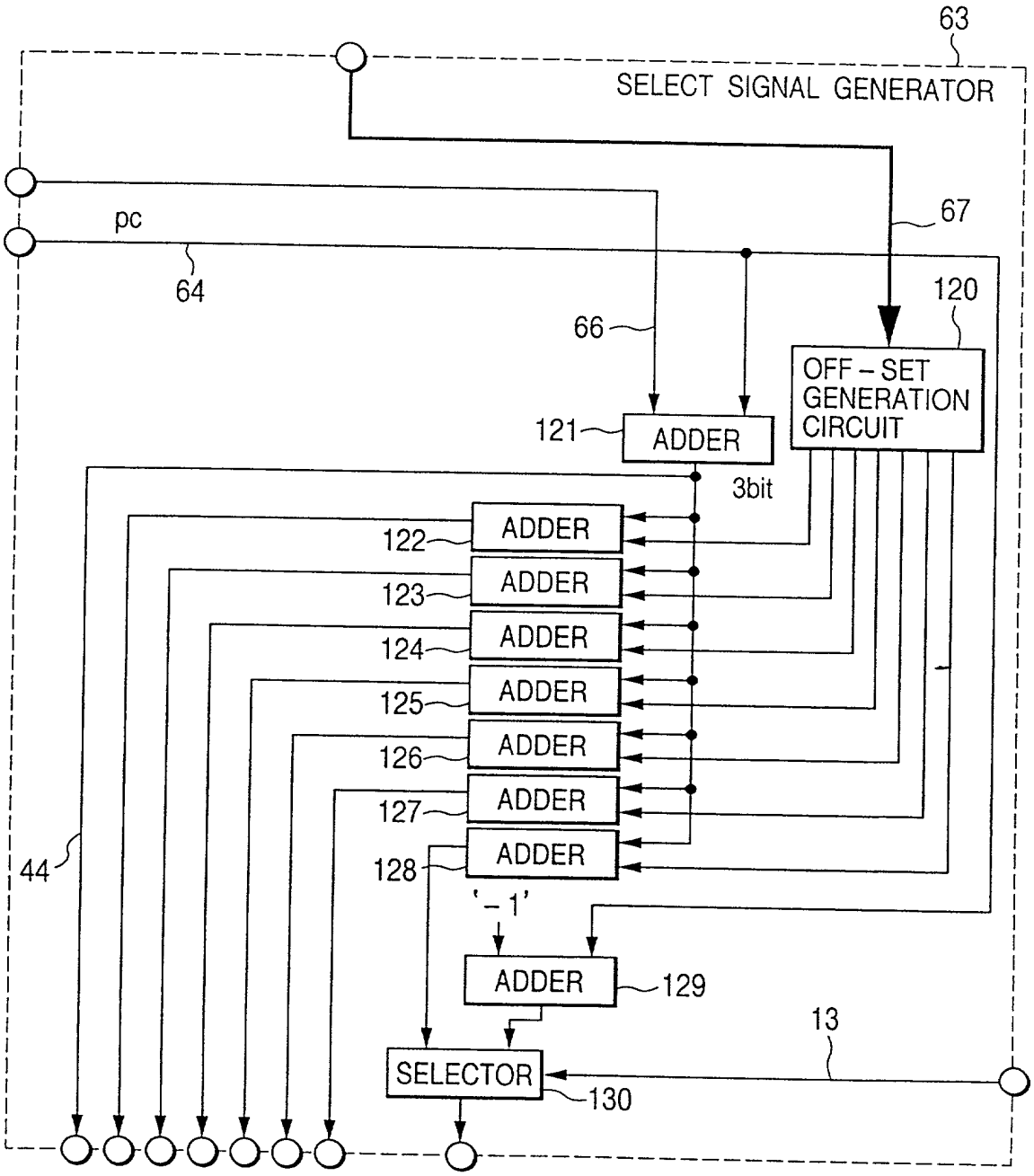

63
SELECT SIGNAL GENERATOR
pc
64
67
66
120
OFF – SET GENERATION CIRCUIT
121
ADDER
3bit
122
ADDER
123
ADDER
124
ADDER
125
ADDER
126
ADDER
127
ADDER
128
ADDER
44
'– 1'
ADDER
129
13
SELECTOR
130

FIG. 15

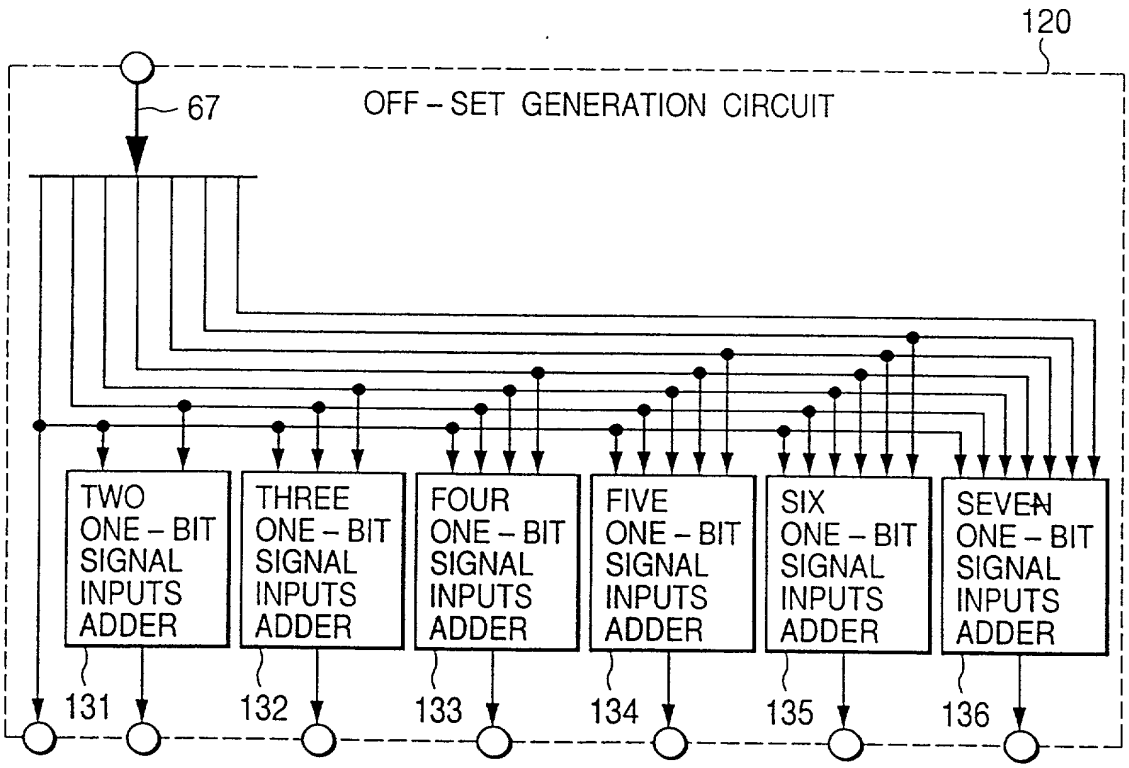

120
67
OFF – SET GENERATION CIRCUIT
TWO ONE – BIT SIGNAL INPUTS ADDER
THREE ONE – BIT SIGNAL INPUTS ADDER
FOUR ONE – BIT SIGNAL INPUTS ADDER
FIVE ONE – BIT SIGNAL INPUTS ADDER
SIX ONE – BIT SIGNAL INPUTS ADDER
SEVEN ONE – BIT SIGNAL INPUTS ADDER
131
132
133
134
135
136

FIG. 16

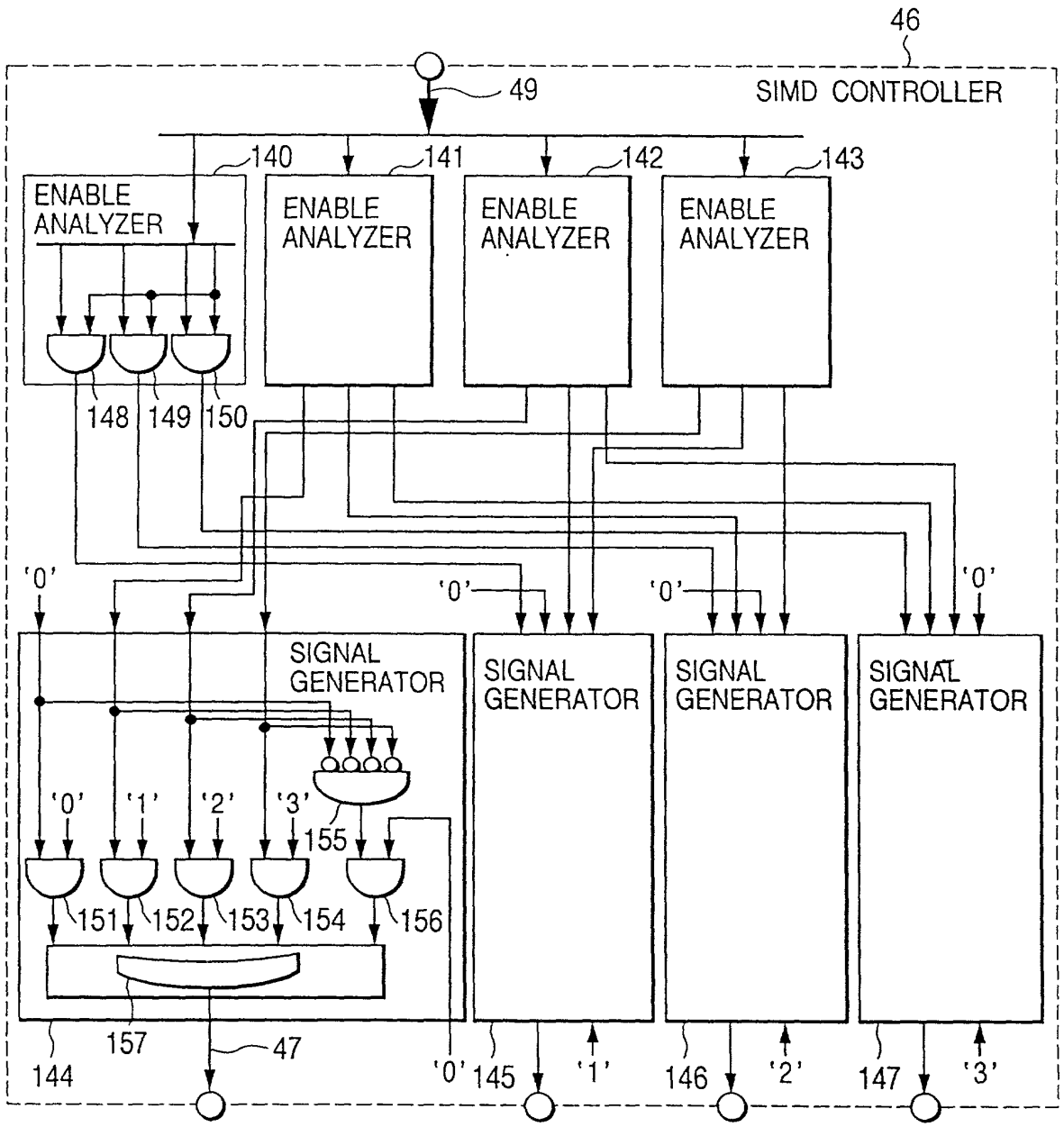

46
49
SIMD CONTROLLER
140
141
142
143
ENABLE ANALYZER
ENABLE ANALYZER
ENABLE ANALYZER
ENABLE ANALYZER
148
149
150
'0'
'0'
'0'
'0'
SIGNAL GENERATOR
SIGNAL GENERATOR
SIGNAL GENERATOR
SIGNAL GENERATOR
'0'
'1'
'2'
'3'
155
151
152
153
154
156
157
47
144
'0'
145
'1'
146
'2'
147
'3'

FIG. 17

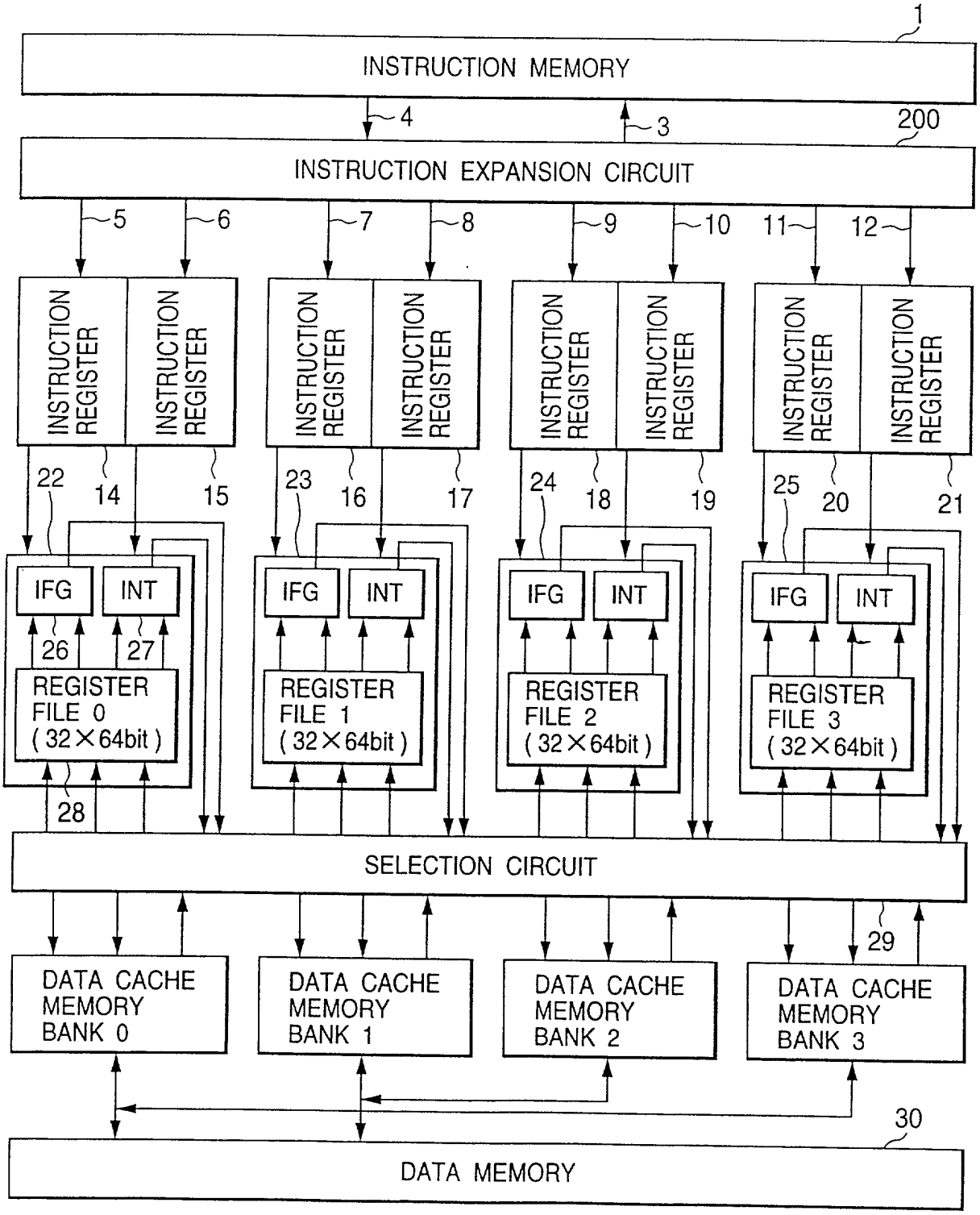
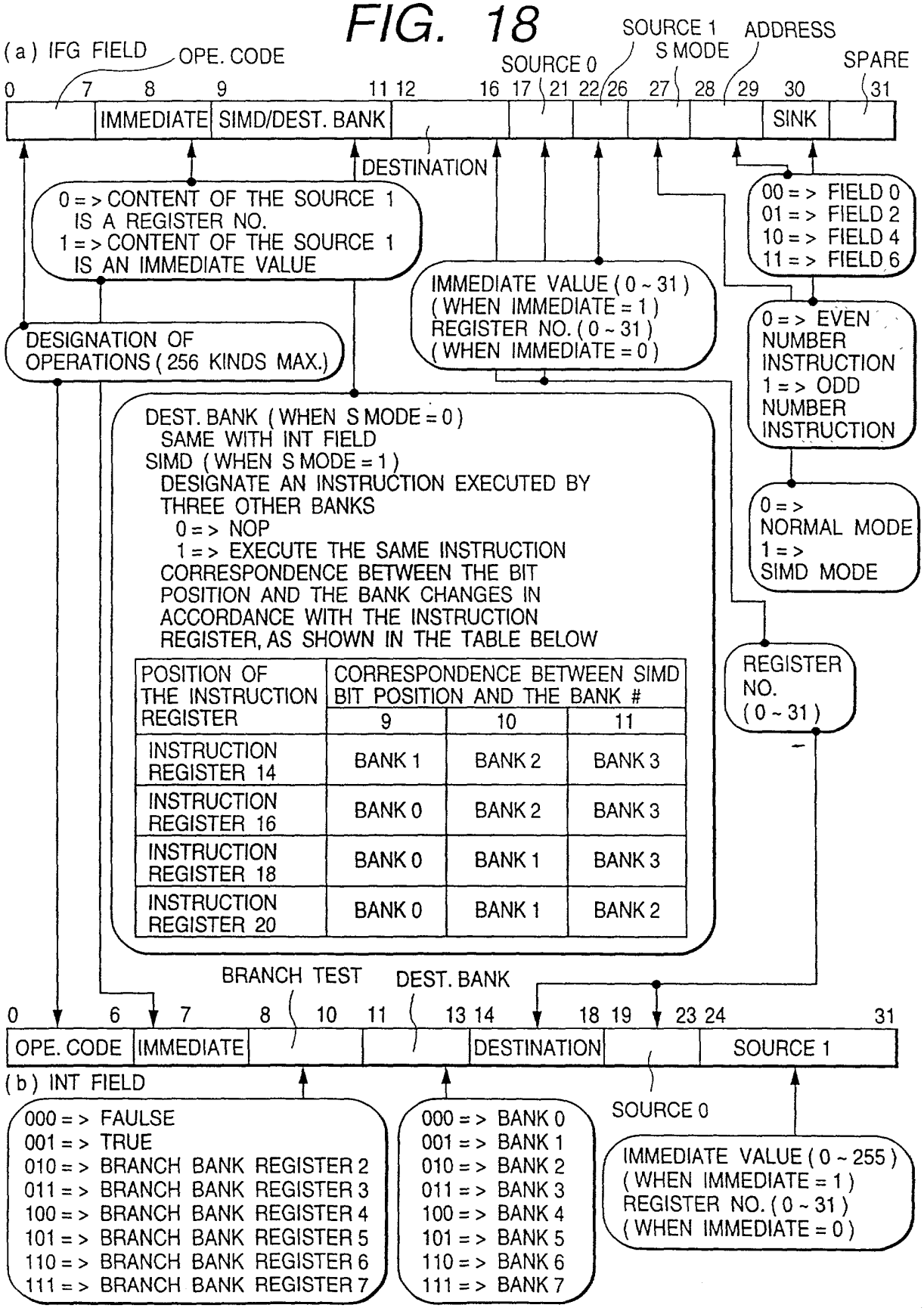

1
INSTRUCTION MEMORY
4
3
200
INSTRUCTION EXPANSION CIRCUIT
5
6
7
8
9
10
11
12
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
22
14
15
23
16
17
24
18
19
25
20
21
IFG
INT
IFG
INT
IFG
INT
IFG
INT
26
27
REGISTER FILE 0 (32×64bit)
REGISTER FILE 1 (32×64bit)
REGISTER FILE 2 (32×64bit)
REGISTER FILE 3 (32×64bit)
28
SELECTION CIRCUIT
29
DATA CACHE MEMORY BANK 0
DATA CACHE MEMORY BANK 1
DATA CACHE MEMORY BANK 2
DATA CACHE MEMORY BANK 3
30
DATA MEMORY

FIG. 18



POSITION OF THE INSTRUCTION REGISTER	CORRESPONDENCE BETWEEN SIMD BIT POSITION AND THE BANK #		
	9	10	11
INSTRUCTION REGISTER 14	BANK 1	BANK 2	BANK 3
INSTRUCTION REGISTER 16	BANK 0	BANK 2	BANK 3
INSTRUCTION REGISTER 18	BANK 0	BANK 1	BANK 3
INSTRUCTION REGISTER 20	BANK 0	BANK 1	BANK 2

FIG. 19

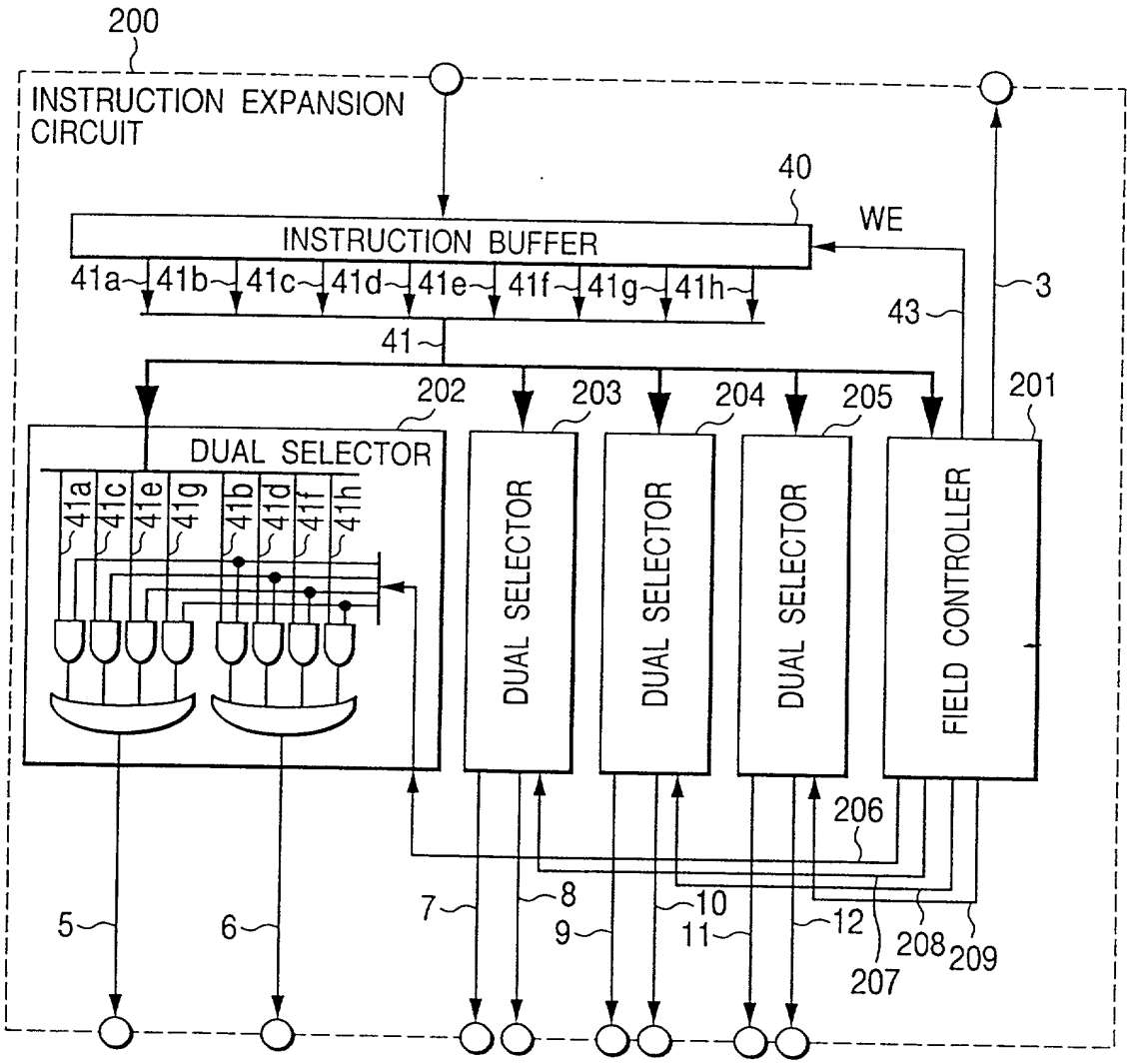

200
INSTRUCTION EXPANSION CIRCUIT
40
WE
INSTRUCTION BUFFER
41a
41b
41c
41d
41e
41f
41g
41h
43
3
41
202
203
204
205
201
DUAL SELECTOR
41a
41c
41e
41g
41b
41d
41f
41h
DUAL SELECTOR
DUAL SELECTOR
DUAL SELECTOR
FIELD CONTROLLER
206
5
6
7
8
9
10
11
12
207
208
209

FIG. 20

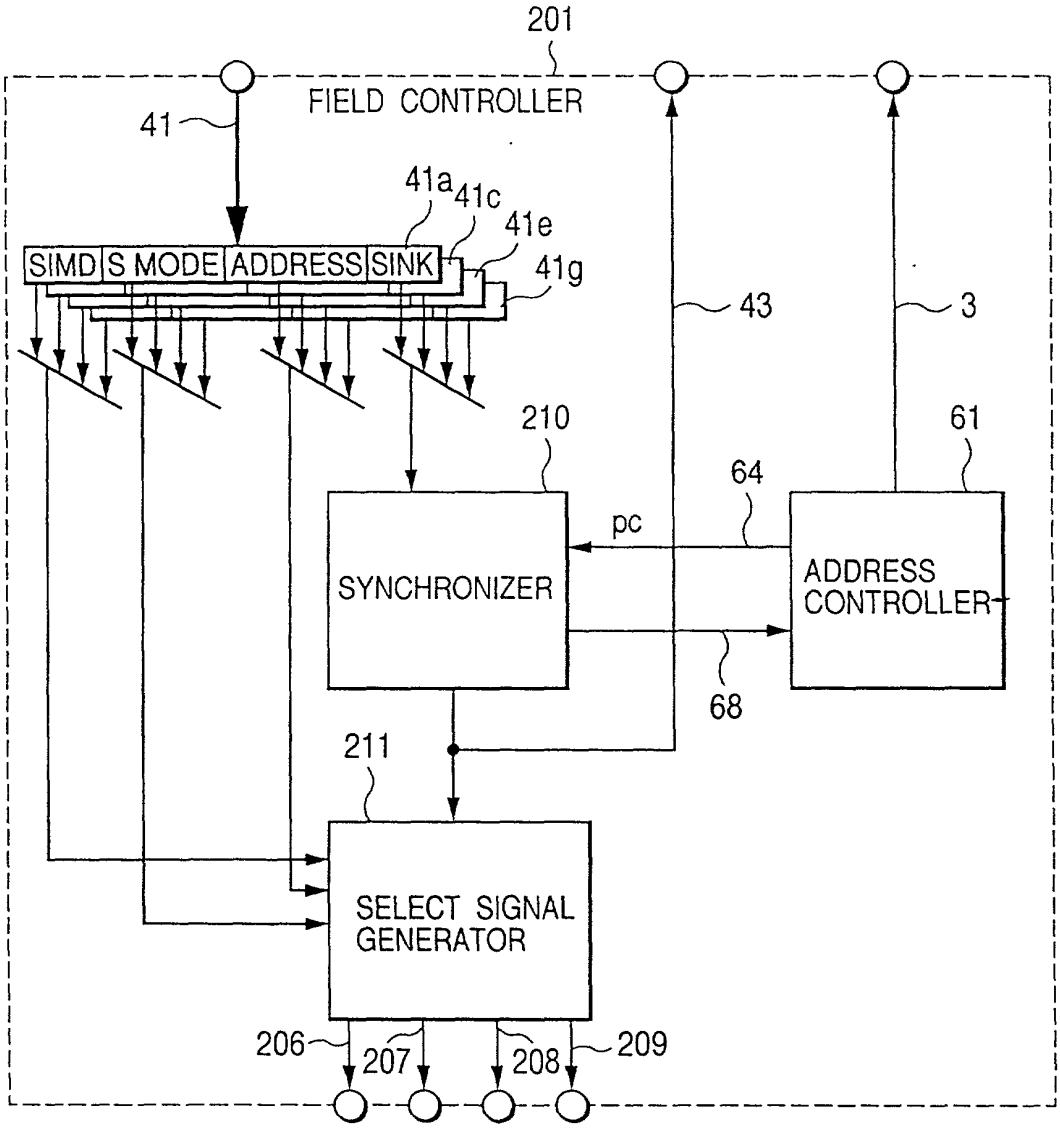

201
FIELD CONTROLLER
41
41a
41c
41e
41g
SIMD
S MODE
ADDRESS
SINK
43
3
210
61
64
pc
SYNCHRONIZER
ADDRESS CONTROLLER
68
211
SELECT SIGNAL GENERATOR
206
207
208
209

FIG. 21

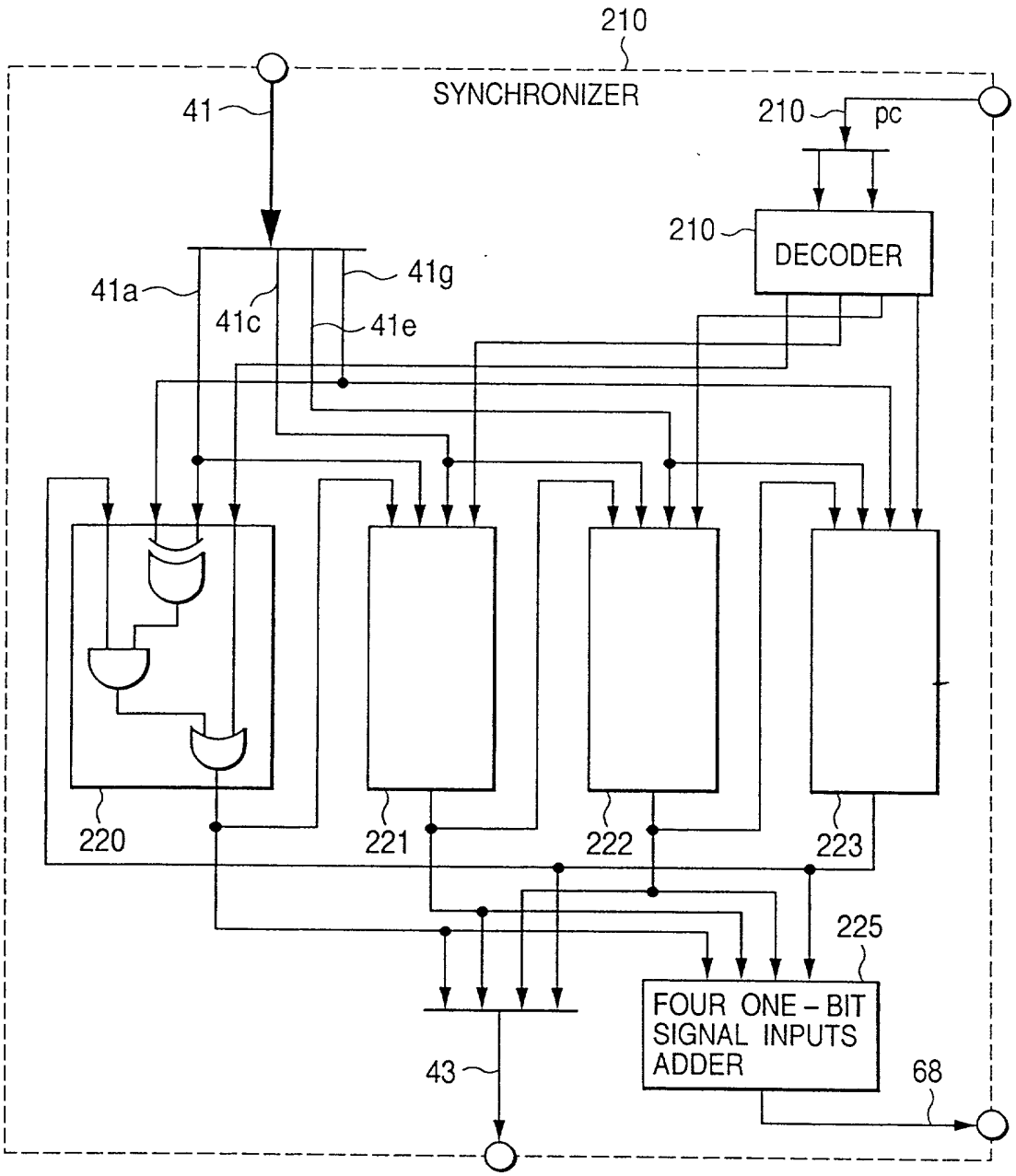

210
SYNCHRONIZER
41
210
pc
210
DECODER
41a
41c
41g
41e
220
221
222
223
225
FOUR ONE-BIT SIGNAL INPUTS ADDER
43
68

FIG. 22

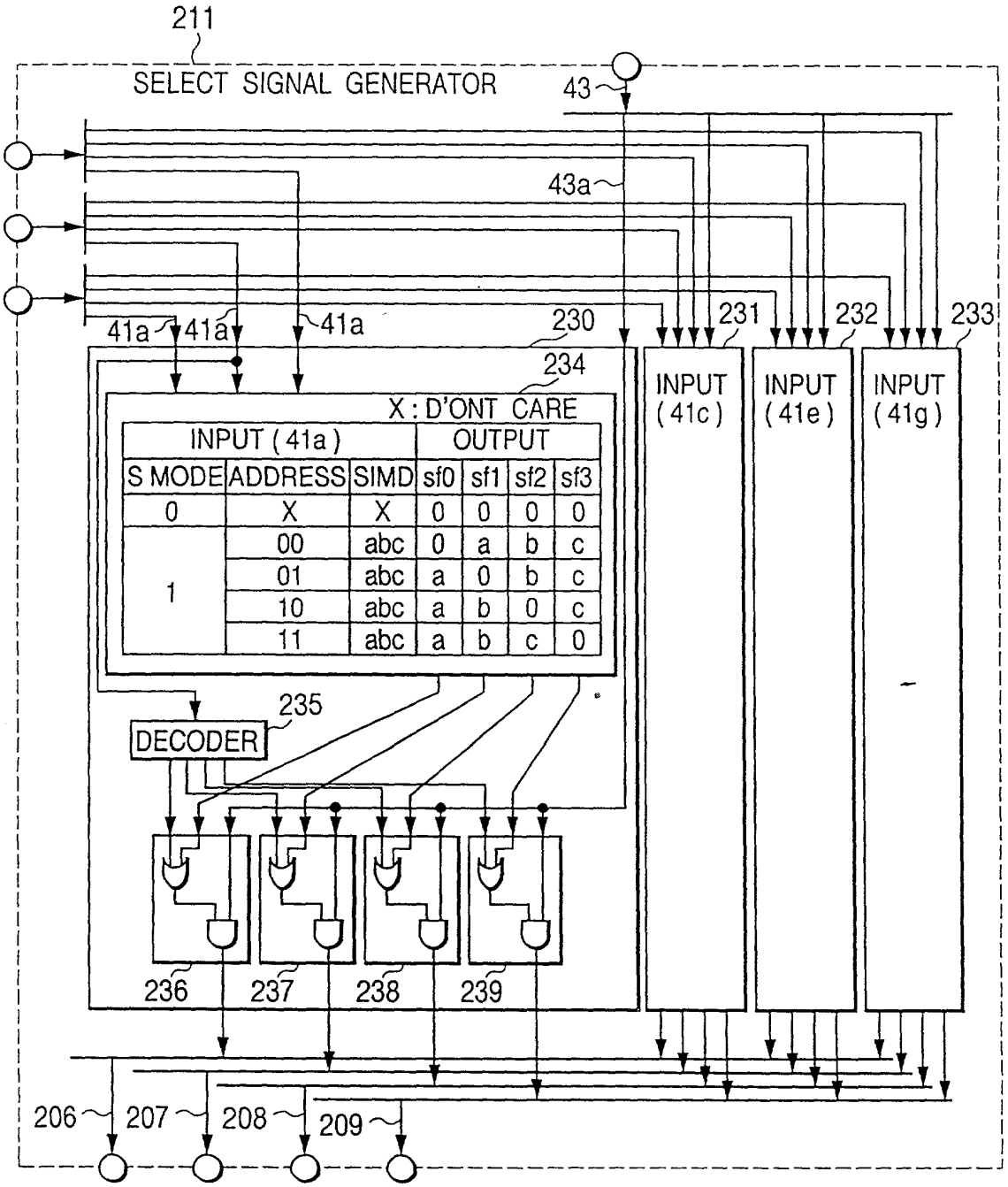

211
SELECT SIGNAL GENERATOR
43
43a
41a
41a
41a
230
231
232
233
234
X : D'ONT CARE
INPUT (41a)
OUTPUT
S MODE
ADDRESS
SIMD
sf0
sf1
sf2
sf3
0
X
X
0
0
0
0
1
00
abc
0
a
b
c
01
abc
a
0
b
c
10
abc
a
b
0
c
11
abc
a
b
c
0
INPUT (41c)
INPUT (41e)
INPUT (41g)
235
DECODER
236
237
238
239
206
207
208
209

FIG. 23

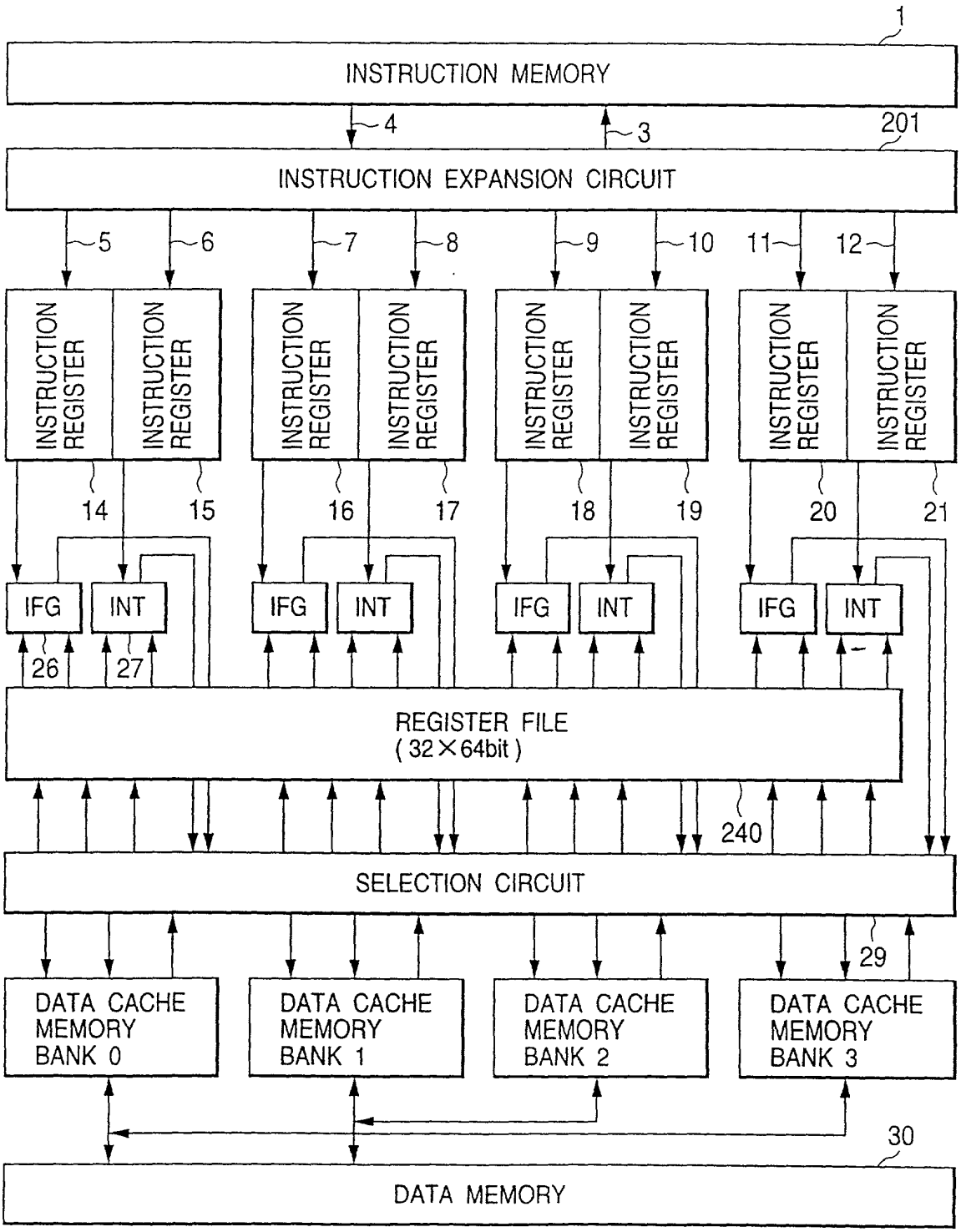
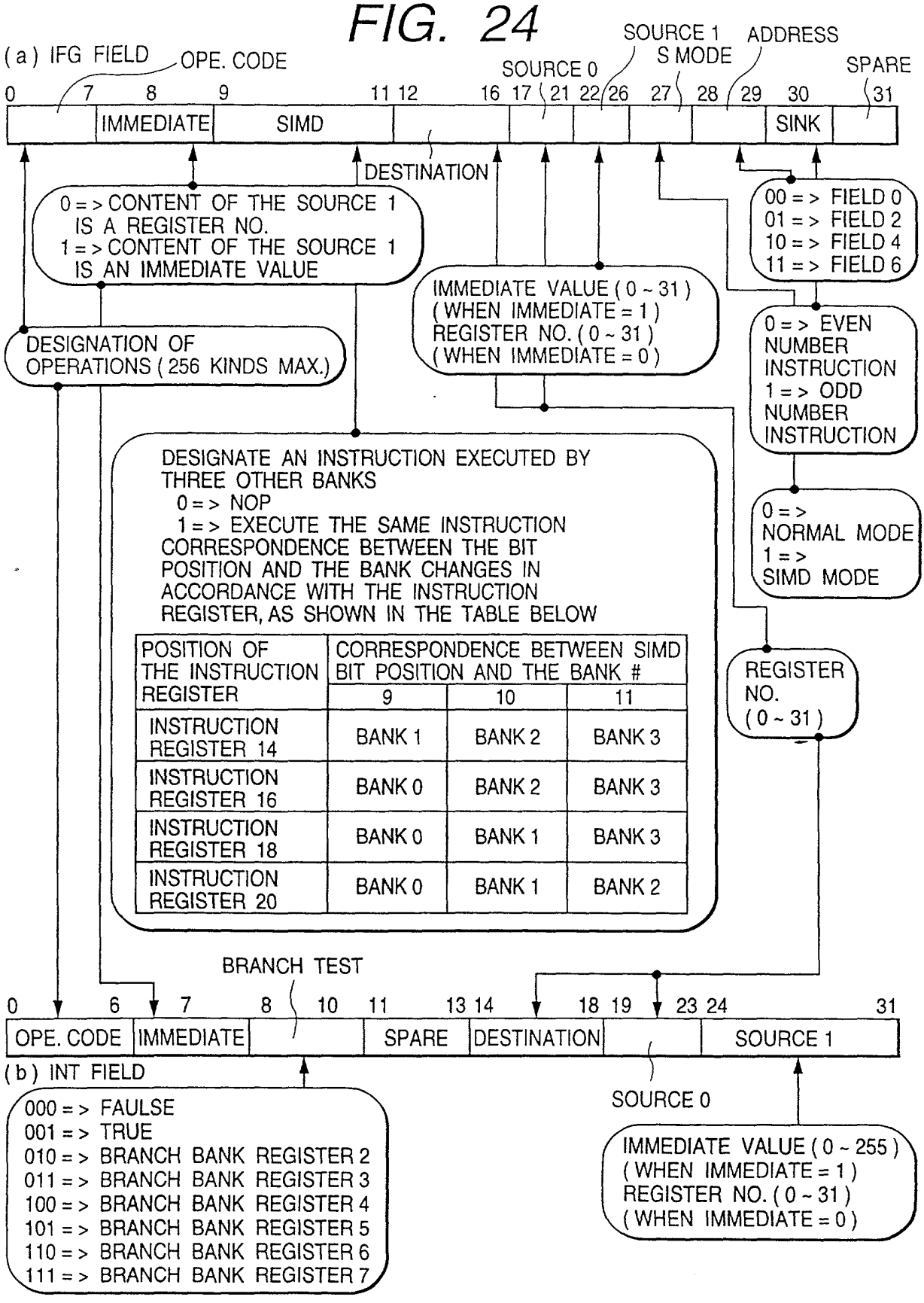

1
INSTRUCTION MEMORY
4
3
201
INSTRUCTION EXPANSION CIRCUIT
5
6
7
8
9
10
11
12
INSTRUCTION REGISTER
14
15
16
17
18
19
20
21
IFG
INT
26
27
REGISTER FILE
(32×64bit)
240
SELECTION CIRCUIT
29
DATA CACHE MEMORY BANK 0
DATA CACHE MEMORY BANK 1
DATA CACHE MEMORY BANK 2
DATA CACHE MEMORY BANK 3
30
DATA MEMORY

FIG. 24



POSITION OF THE INSTRUCTION REGISTER	CORRESPONDENCE BETWEEN SIMD BIT POSITION AND THE BANK #		
	9	10	11
INSTRUCTION REGISTER 14	BANK 1	BANK 2	BANK 3
INSTRUCTION REGISTER 16	BANK 0	BANK 2	BANK 3
INSTRUCTION REGISTER 18	BANK 0	BANK 1	BANK 3
INSTRUCTION REGISTER 20	BANK 0	BANK 1	BANK 2

FIG. 25

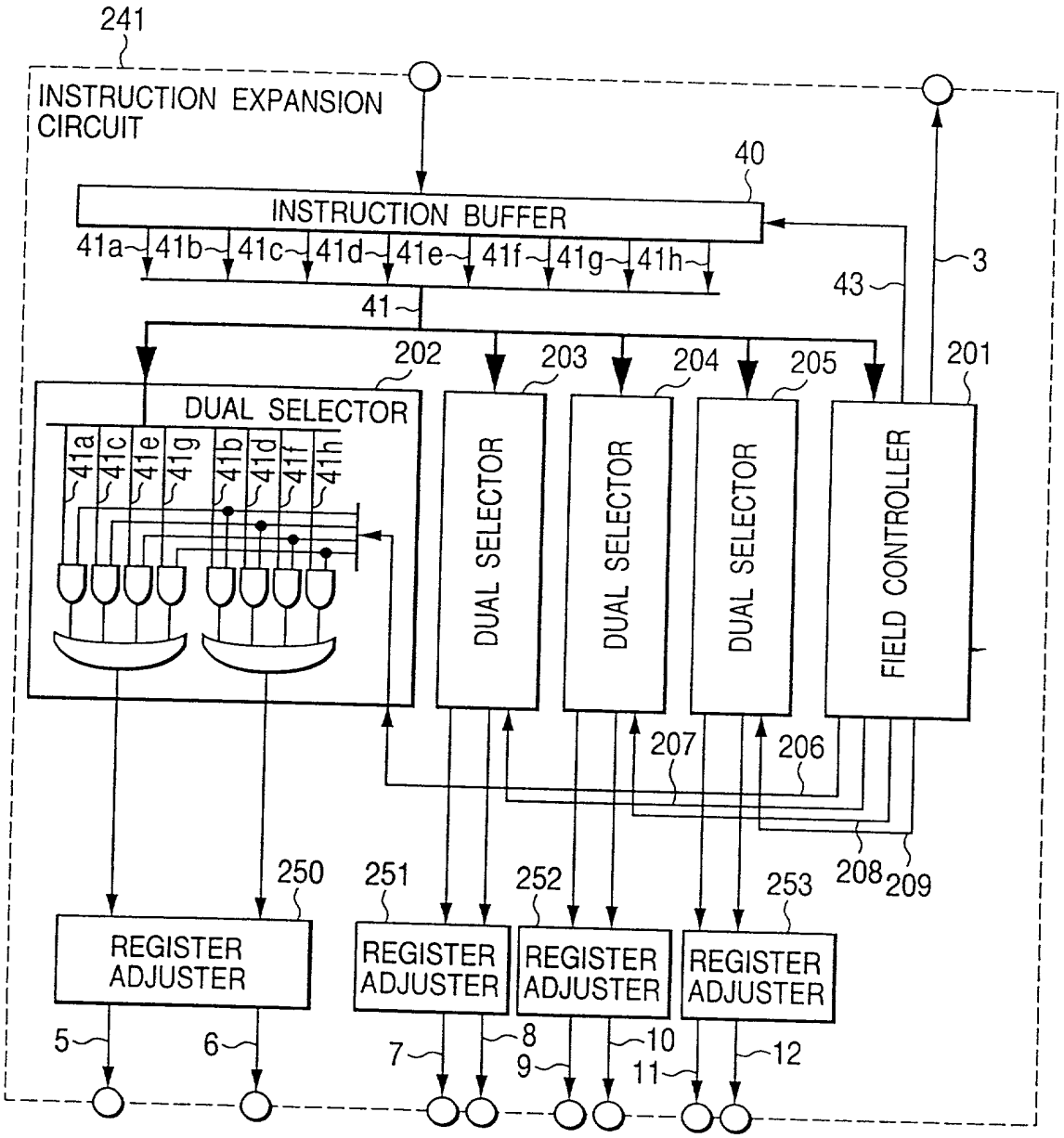

241
INSTRUCTION EXPANSION CIRCUIT
40
INSTRUCTION BUFFER
41a
41b
41c
41d
41e
41f
41g
41h
41
43
3
202
203
204
205
201
DUAL SELECTOR
41a
41c
41e
41g
41b
41d
41f
41h
DUAL SELECTOR
DUAL SELECTOR
DUAL SELECTOR
FIELD CONTROLLER
207
206
208
209
250
251
252
253
REGISTER ADJUSTER
REGISTER ADJUSTER
REGISTER ADJUSTER
REGISTER ADJUSTER
5
6
7
8
9
10
11
12

FIG. 26

INPUT FIELD			OUTPUT FIELD
S MODE	ADDRESS	REGISTER #	REGISTER #
0	X	N	N
1	00	N	N
	01	N	N + 3
	10	N	N + 2
	11	N	N + 1

FIG. 27

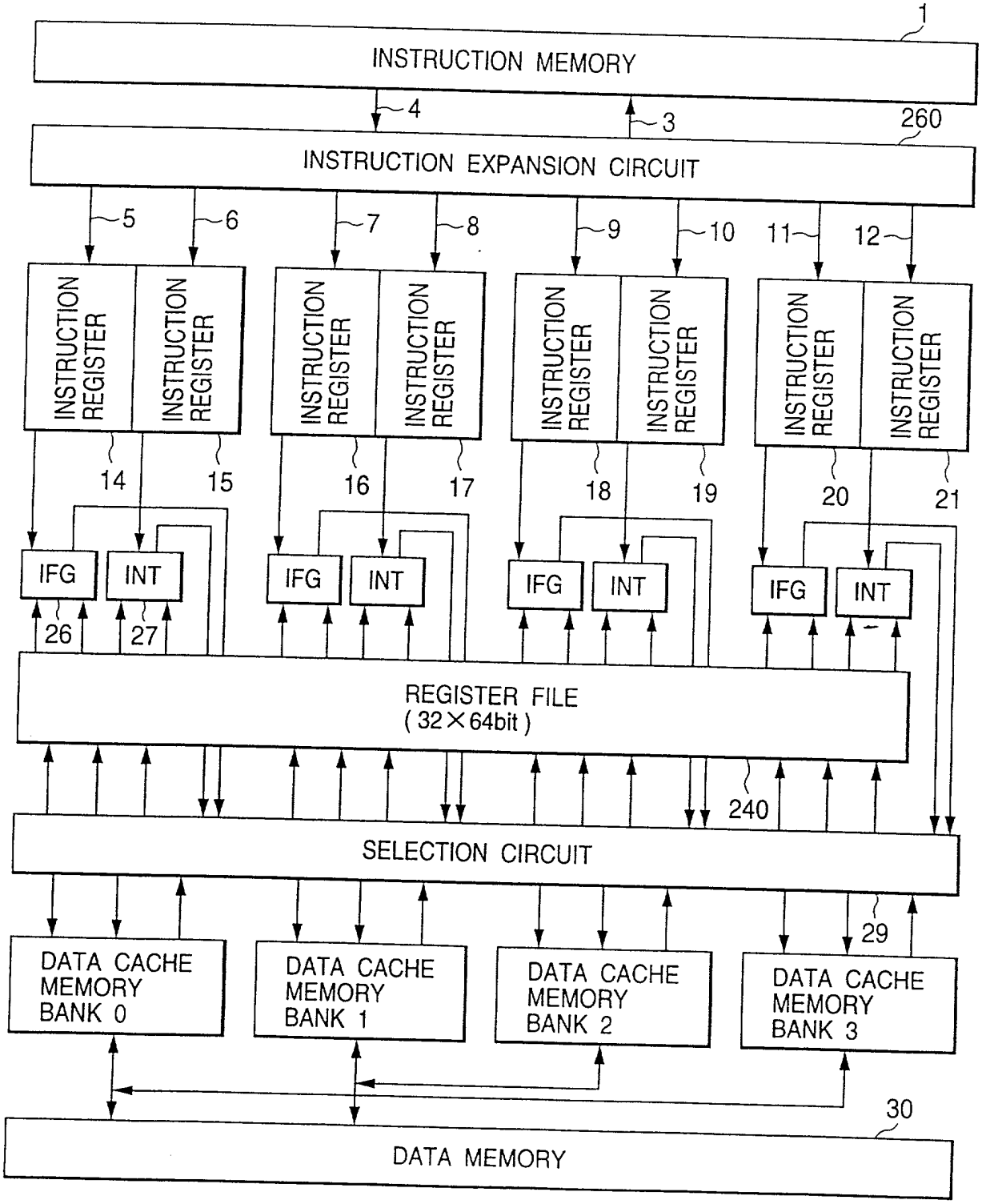
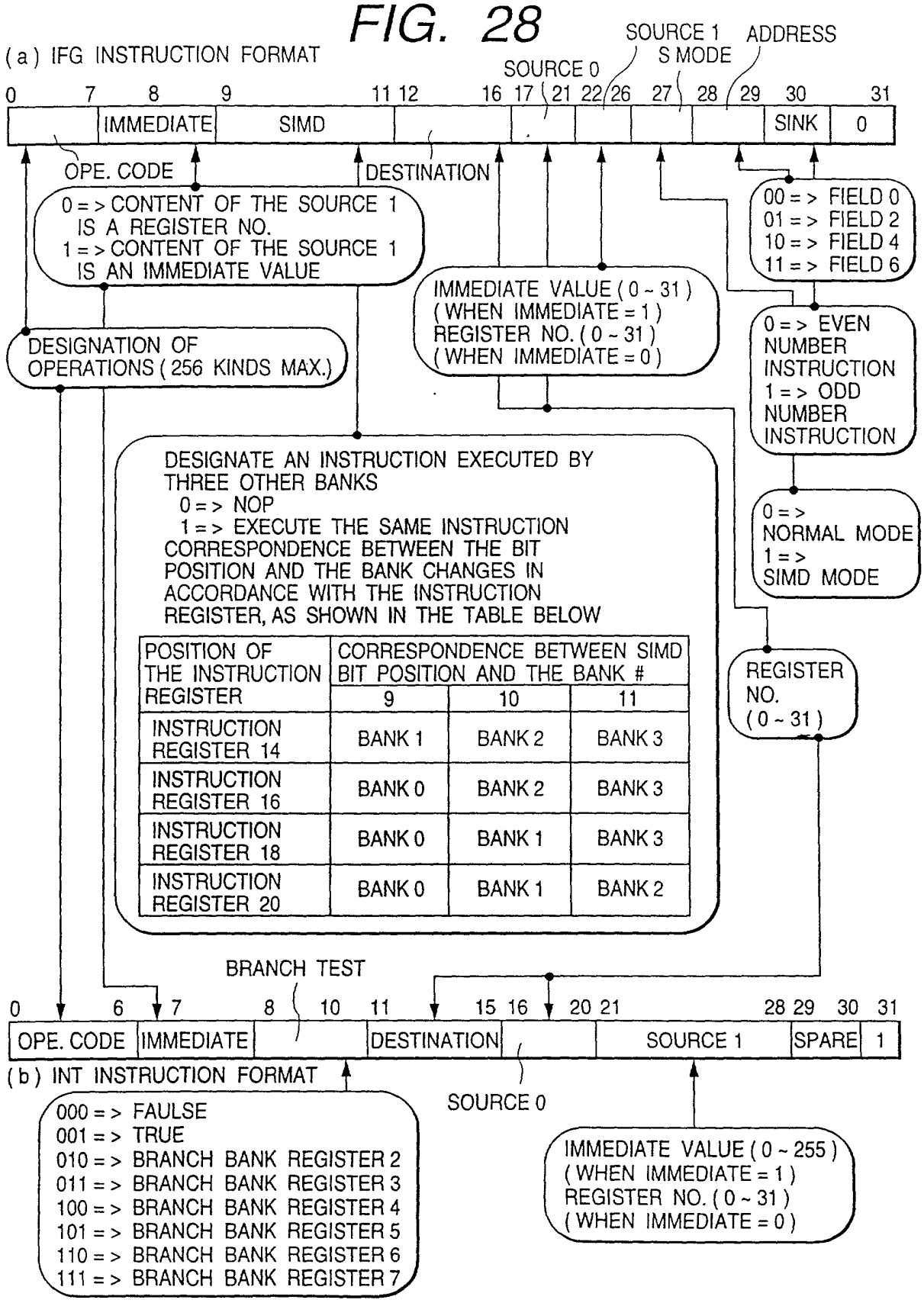

1
INSTRUCTION MEMORY
4
3
260
INSTRUCTION EXPANSION CIRCUIT
5
6
7
8
9
10
11
12
INSTRUCTION REGISTER
14
15
16
17
18
19
20
21
IFG
INT
26
27
REGISTER FILE
(32×64bit)
240
SELECTION CIRCUIT
29
DATA CACHE MEMORY BANK 0
DATA CACHE MEMORY BANK 1
DATA CACHE MEMORY BANK 2
DATA CACHE MEMORY BANK 3
30
DATA MEMORY

FIG. 28



POSITION OF THE INSTRUCTION REGISTER	CORRESPONDENCE BETWEEN SIMD BIT POSITION AND THE BANK #		
	9	10	11
INSTRUCTION REGISTER 14	BANK 1	BANK 2	BANK 3
INSTRUCTION REGISTER 16	BANK 0	BANK 2	BANK 3
INSTRUCTION REGISTER 18	BANK 0	BANK 1	BANK 3
INSTRUCTION REGISTER 20	BANK 0	BANK 1	BANK 2

FIG. 29

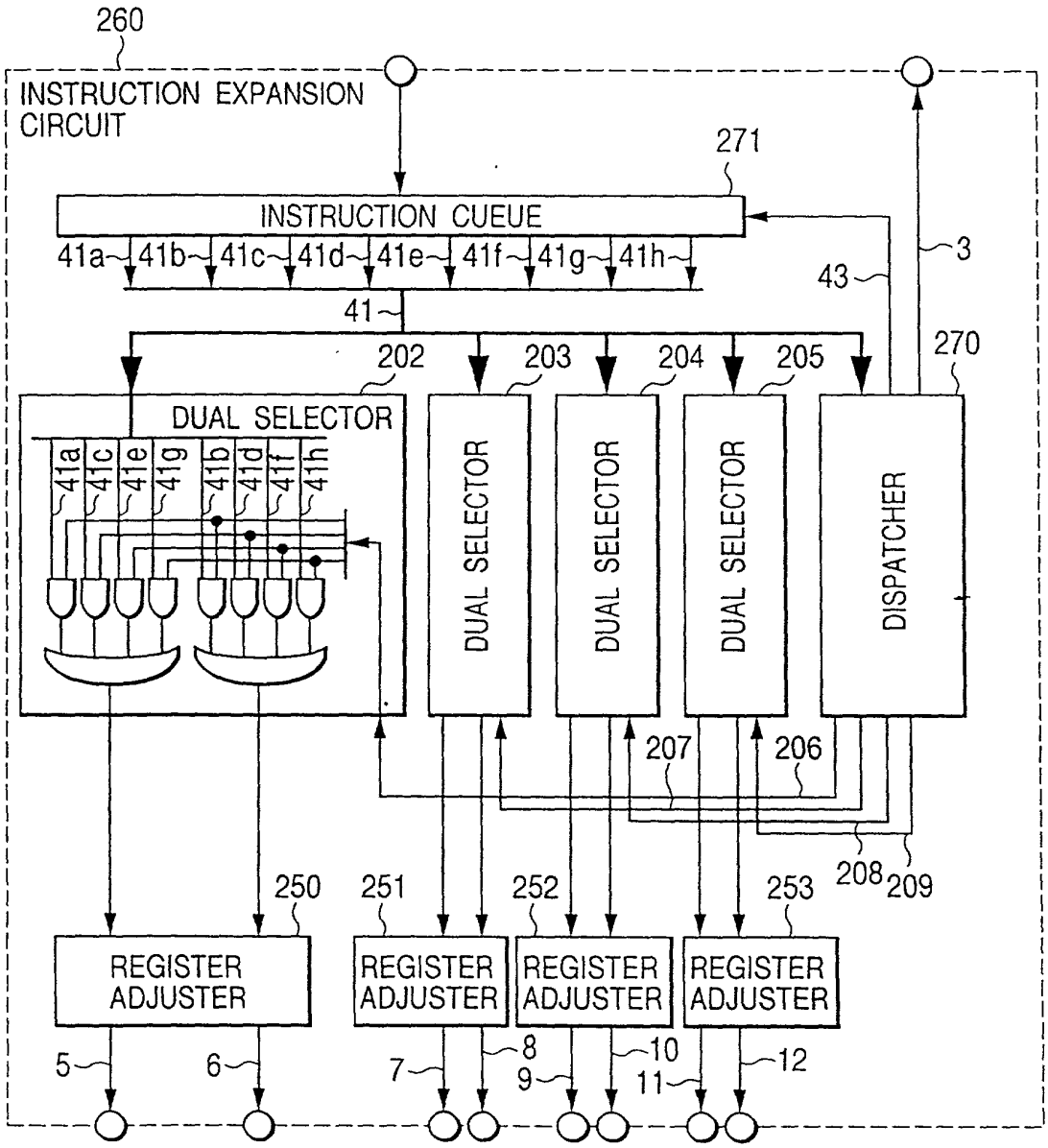
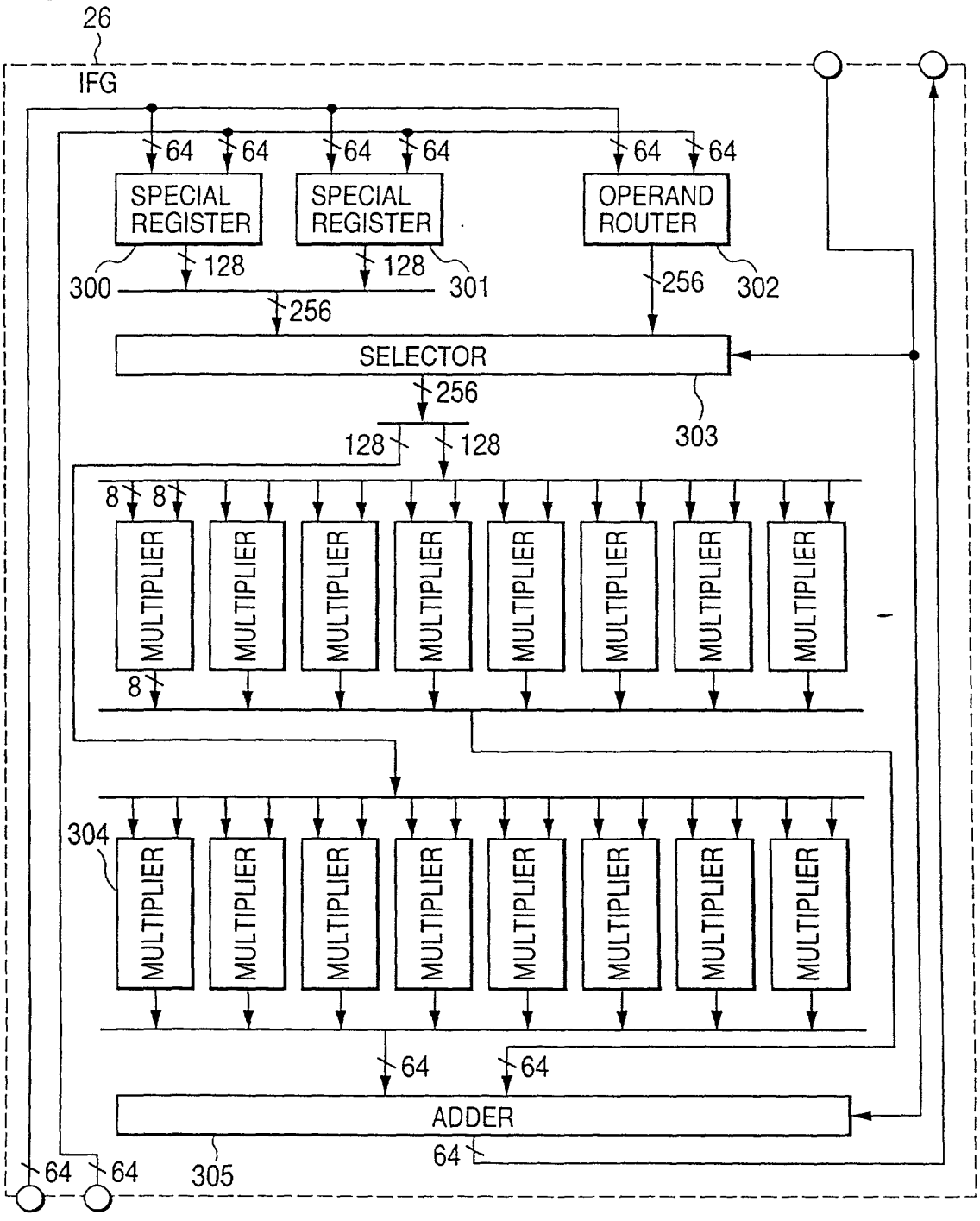

260
INSTRUCTION EXPANSION CIRCUIT
271
INSTRUCTION CUEUE
41a
41b
41c
41d
41e
41f
41g
41h
41
43
3
270
202
203
204
205
DUAL SELECTOR
41a
41c
41e
41g
41b
41d
41f
41h
DUAL SELECTOR
DUAL SELECTOR
DUAL SELECTOR
DISPATCHER
207
206
208
209
250
251
252
253
REGISTER ADJUSTER
REGISTER ADJUSTER
REGISTER ADJUSTER
REGISTER ADJUSTER
5
6
7
8
9
10
11
12

FIG. 30


26
IFG
64
64
64
64
64
64
SPECIAL REGISTER
SPECIAL REGISTER
OPERAND ROUTER
128
128
300
301
256
256
302
SELECTOR
256
303
128
128
8
8
MULTIPLIER
8
304
64
64
ADDER
64
64
64
305